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Triathlon

Compal confidential

Schematics Document

Mobile Yonah uFCPGA with Intel Calistoga_GM/PM+ICH7-M core logic

星期三, 七月 12, 2006

REV:0.3

Security Classification	Compal Secret Data		
Issued Date	2005/10/06	Deciphered Date	2006/10/06

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File Name : LA-3281P

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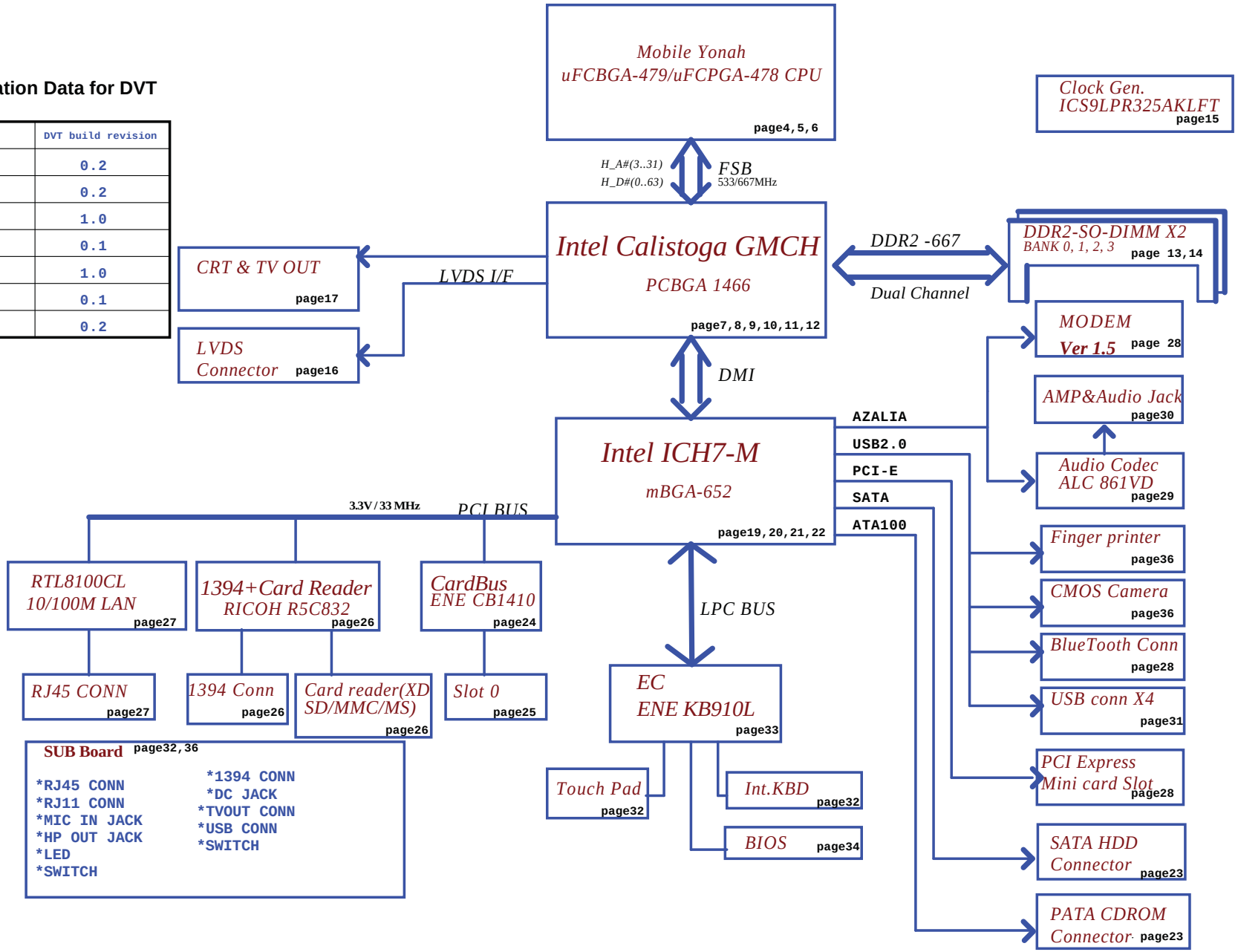
ZZZ1

14W_PCB

HDL20 PCB panelization Data for DVT

PCB Function	PCB Number	DVT build revision
MB	LA3281P	0.2
Audio/USB	LS3251P	0.2
SW board	LS3102P	1.0
CRT board	LS3253P	0.1
TP board	LS3104P	1.0
FP Board	LS3255P	0.1
LED board	LS3256P	0.2



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Voltage Rails

power plane / State	+B LDO3 LDO5	+5VALW +3VALW	+1.8V +5V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.2VS +VGA_CORE +0.9VS +CPU_CORE +VCCP
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

O MEANS ON
X MEANS OFF

S3 : STR
S4 : STD
S5 : SOFT OFF

SKU ID Table

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
* 0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

SKU ID	MB ID(H)	MB ID(L)
0		
1		
2		
3	HDL10	HDL00
* 4		HDL20
5	IDL12	HDL30
6		
7		

	MB ID
H	15"
L	14"

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
1394	AD22	0	PIRQG/H
LAN	AD17	3	PIRQF
CardBus	AD20	2	PIRQA

BOM Structure

MARK	FUNCTION
@	NC FOR ALL
GIGA@	8110SBL(SCL)Giga LAN
10/100@	8100CL 10/100Mb LAN
UMA@	Internal 945GM
VGA@	External G7xM

USB PORT LIST

PORT	DEVICE
0	LEFT SIDE
1	BT(HDL00/10)
2	RIGHT SIDE
3	CMOS
4	RIGHT SIDE
5	FINGER PRINTER
6	RIGHT SIDE
7	BT(HDL20)

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b

EC SM Bus2 address

Device	Address
ADM1032	1001 100X b

ICH6 SM Bus address

Device	Address
Clock Generator (ICS954226)	1101 001Xb
DDRII DIMM0	1010 000Xb
DDRII DIMM1	1010 010Xb

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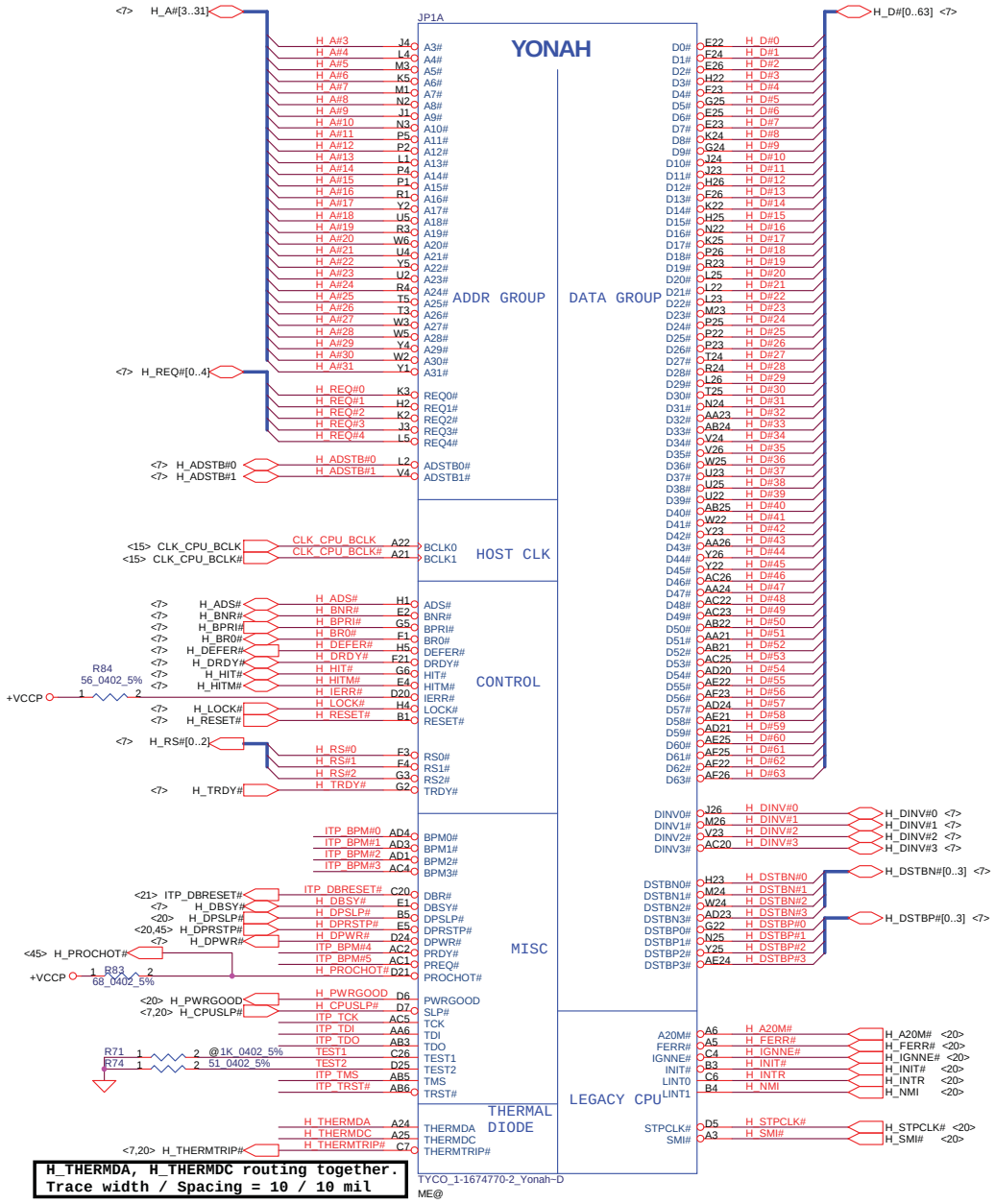
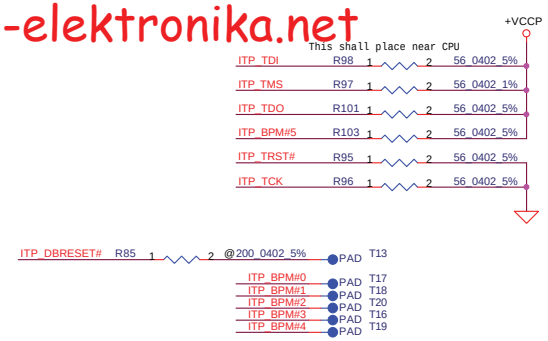
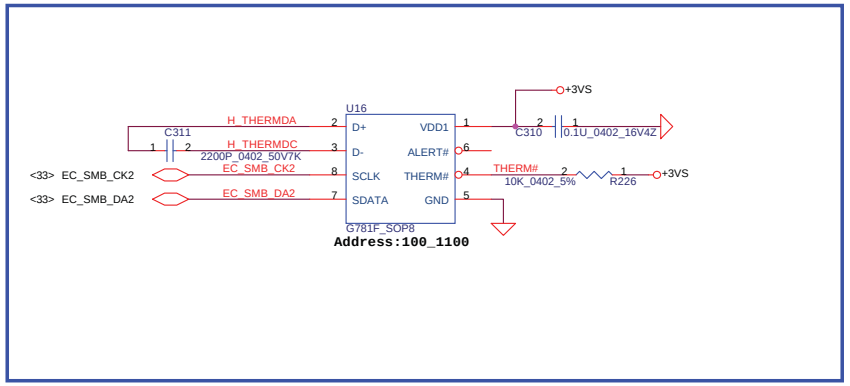
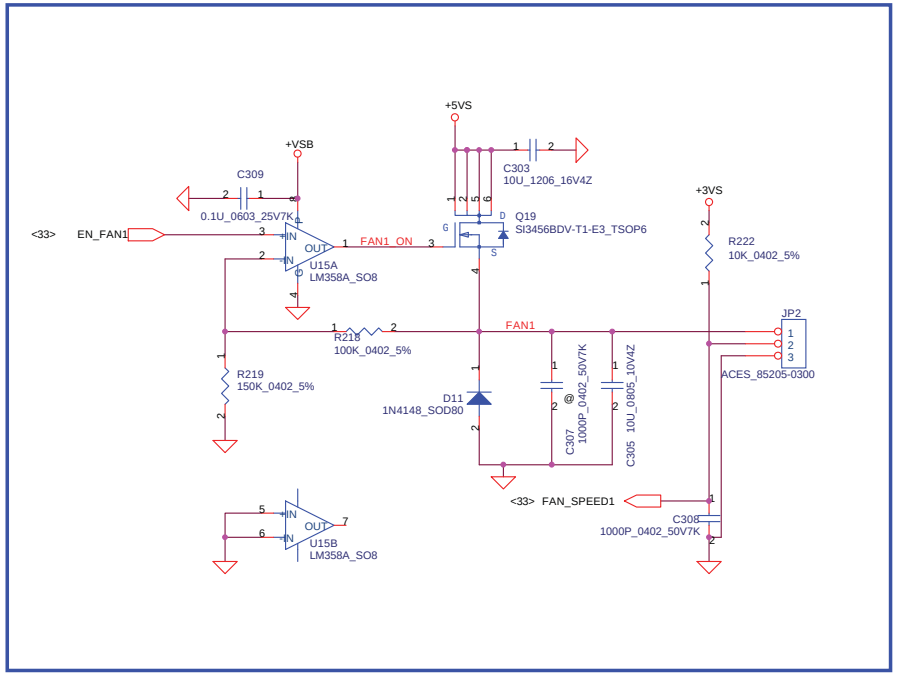
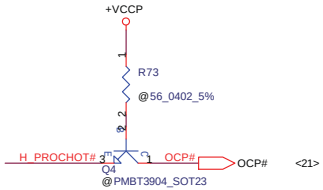


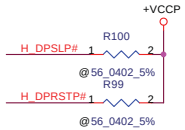
H_THERMDA, H_THERMDC routing together.
Trace width / Spacing = 10 / 10 mil











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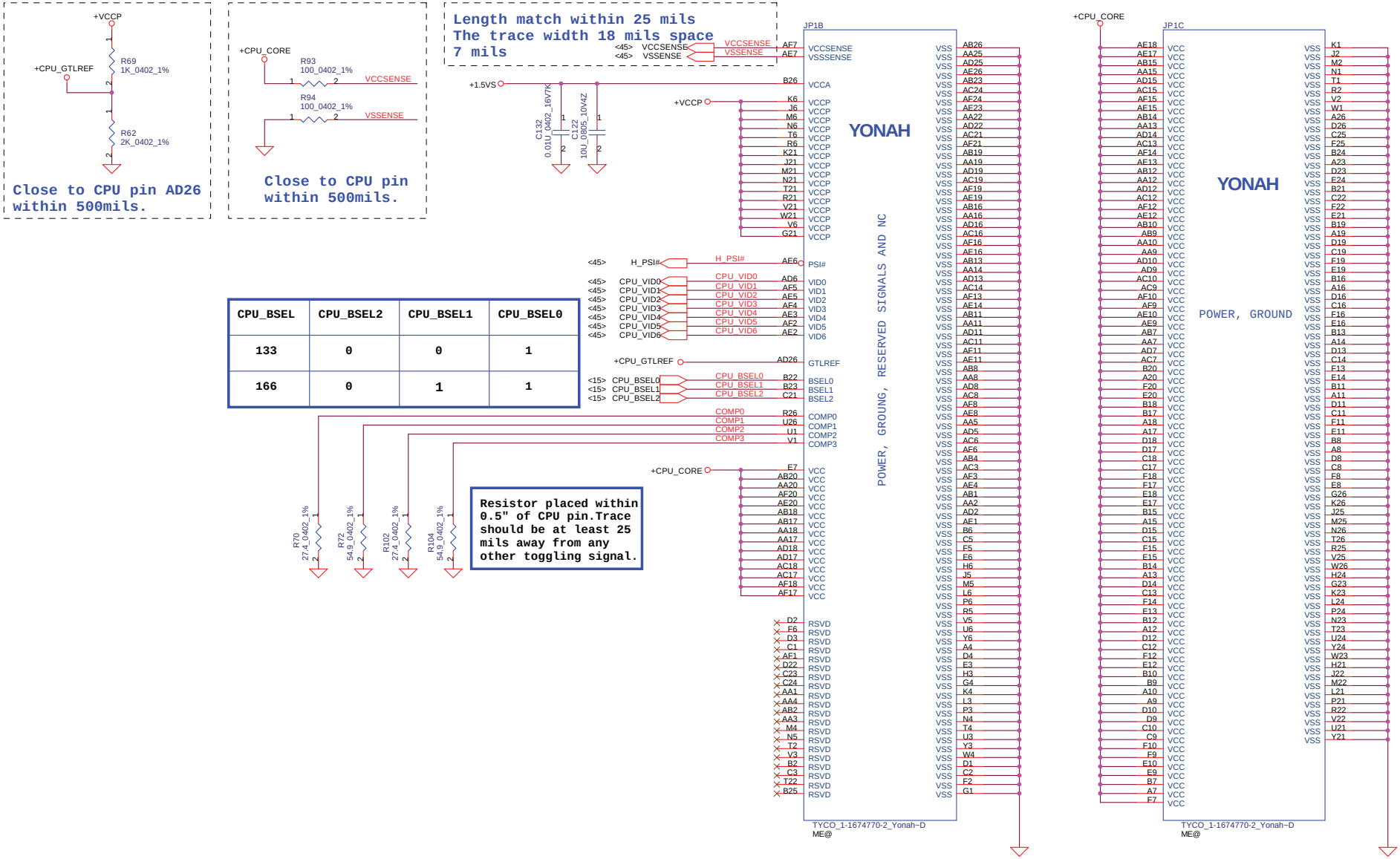

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1

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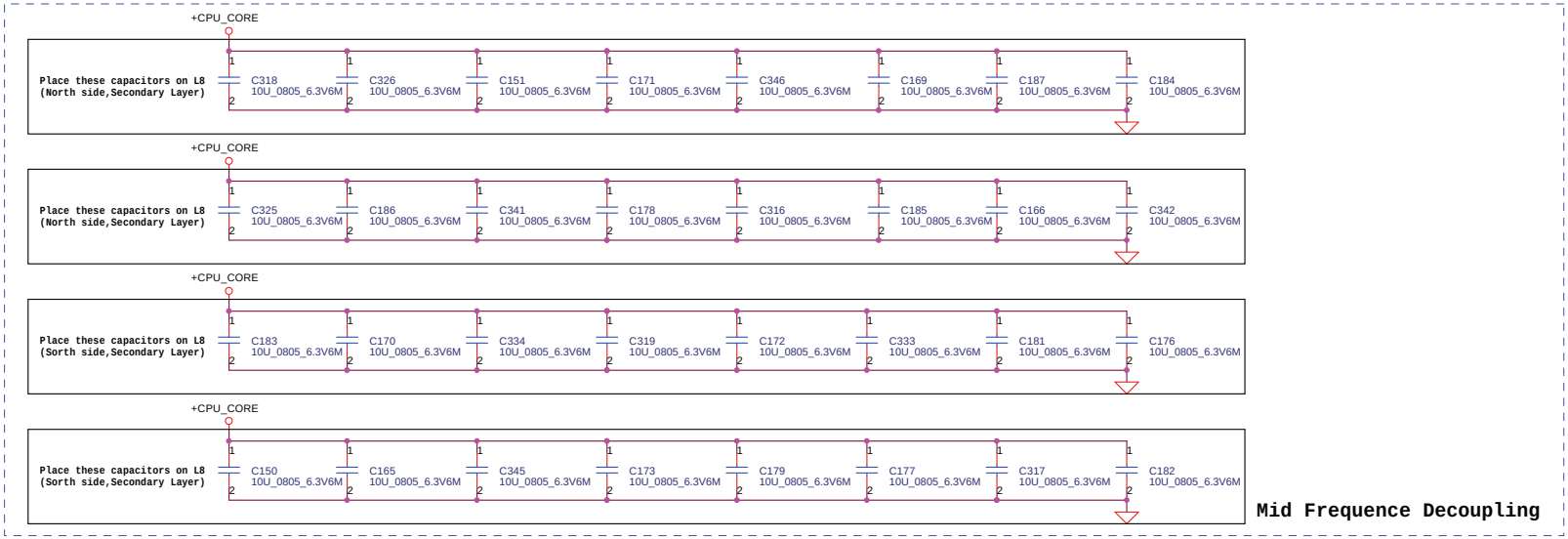
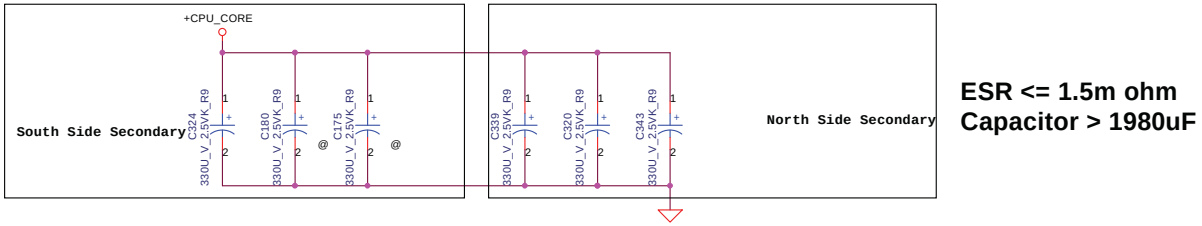
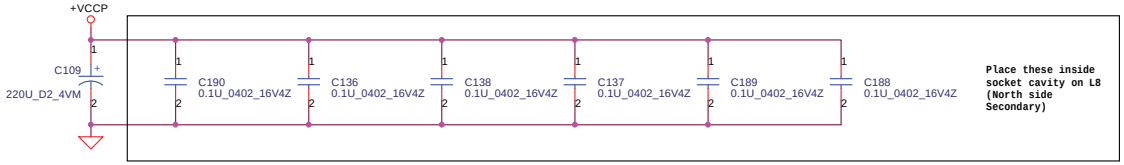




ESR <= 1.5m ohm
Capacitor > 1980uF



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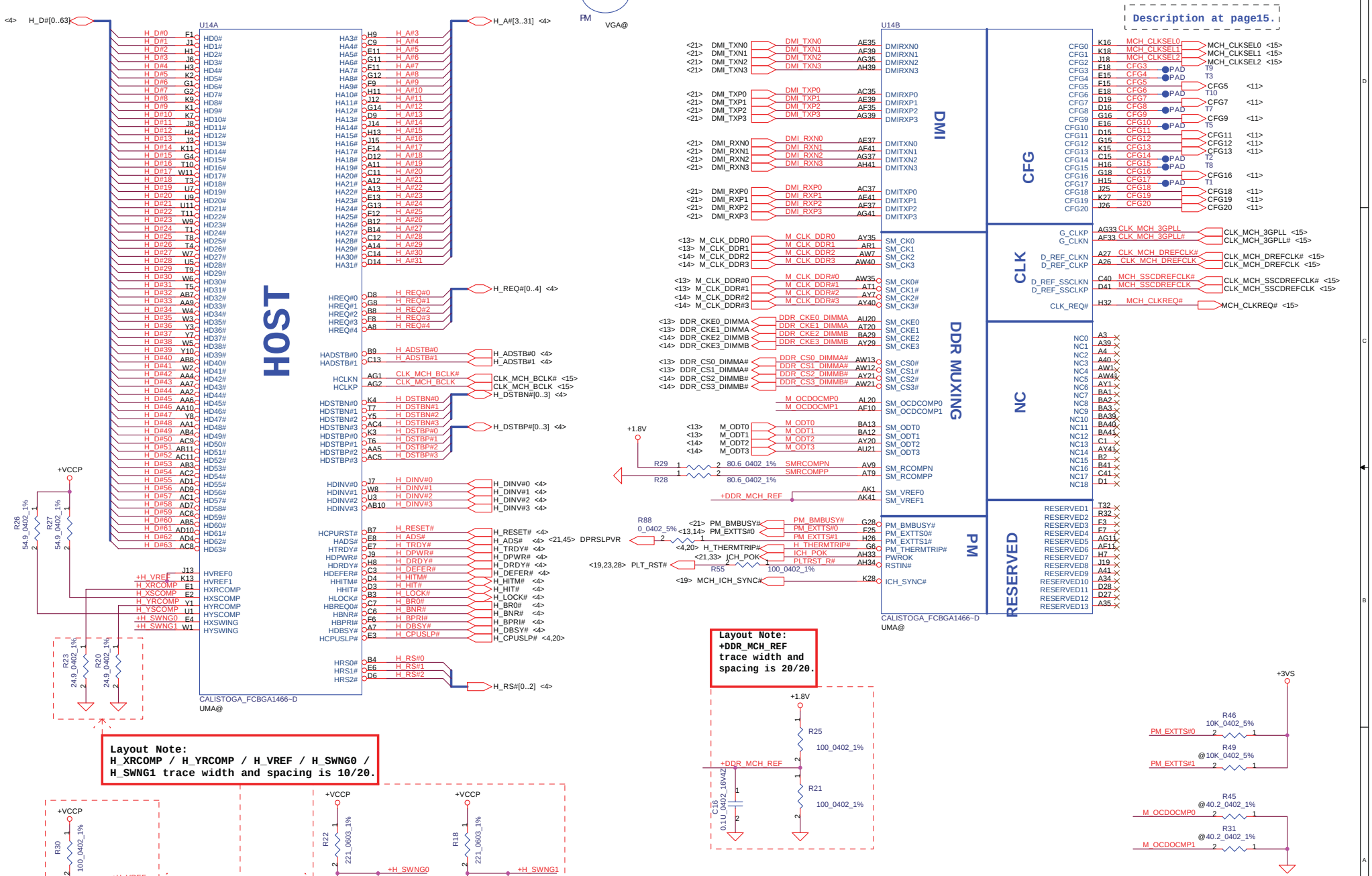

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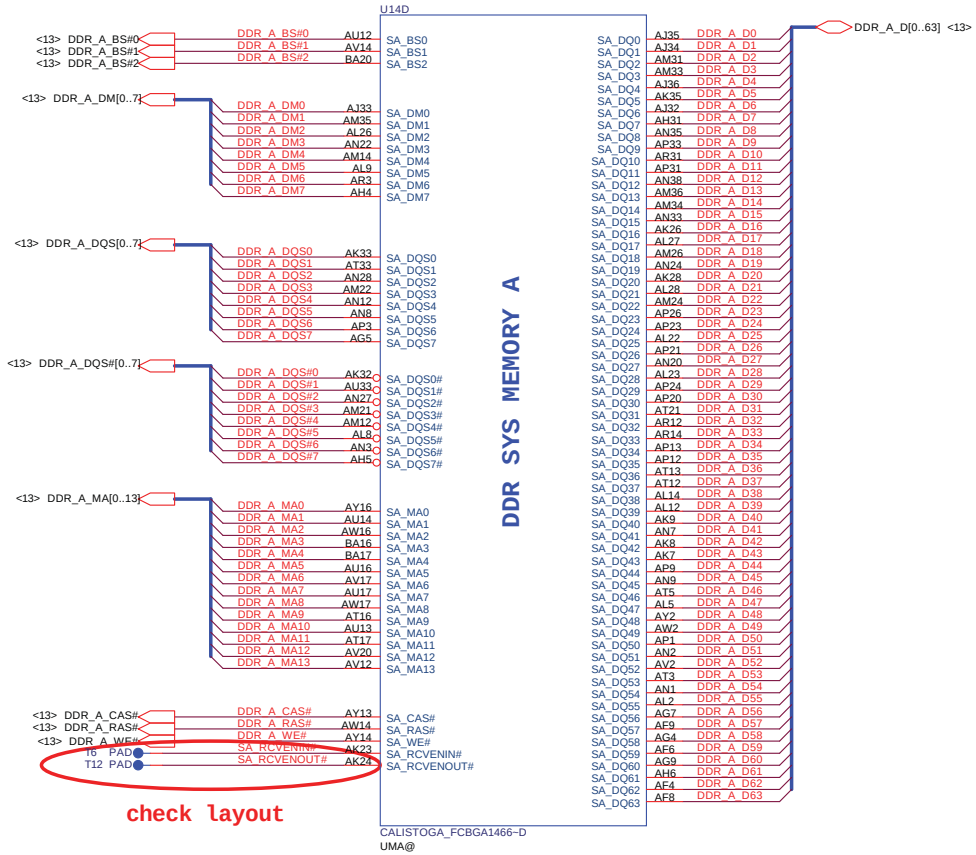

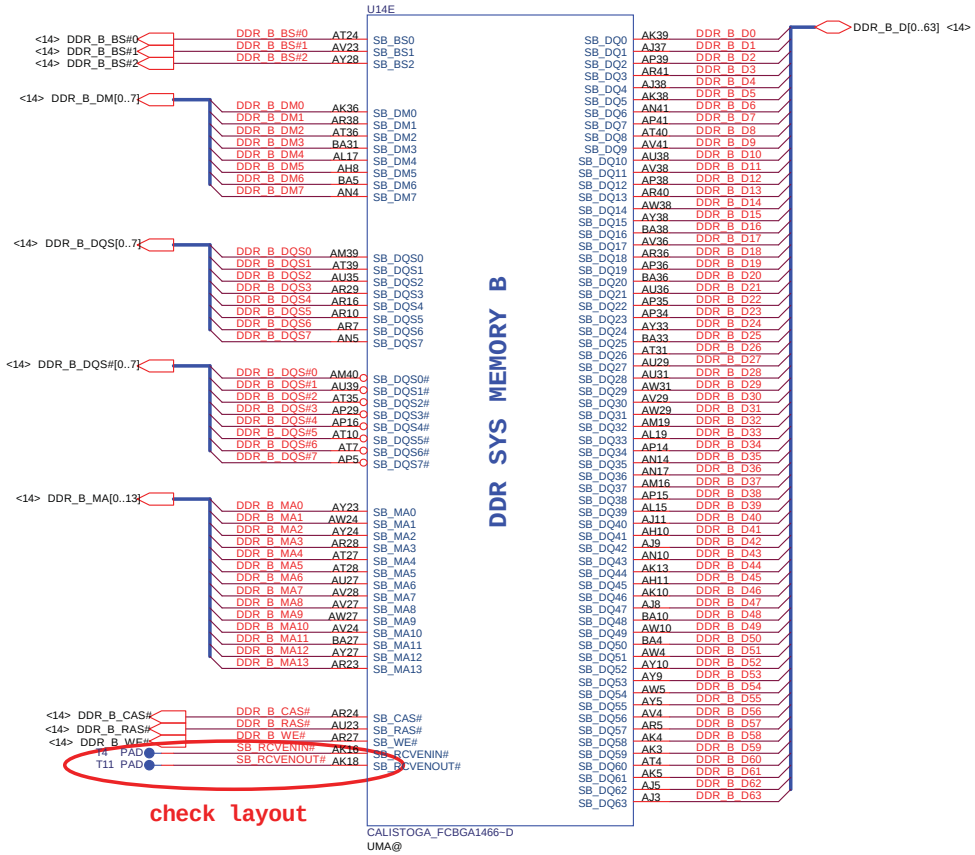

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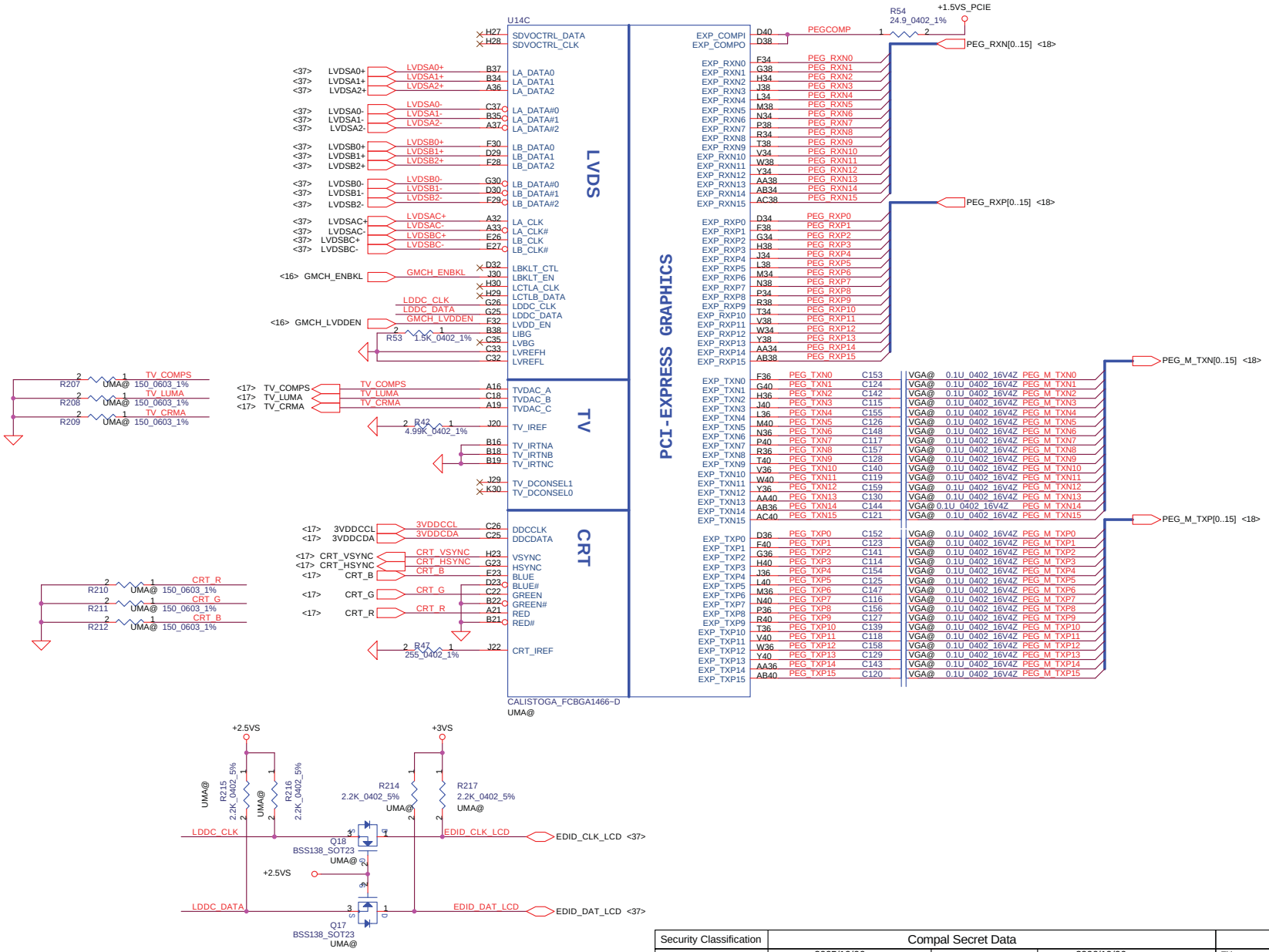

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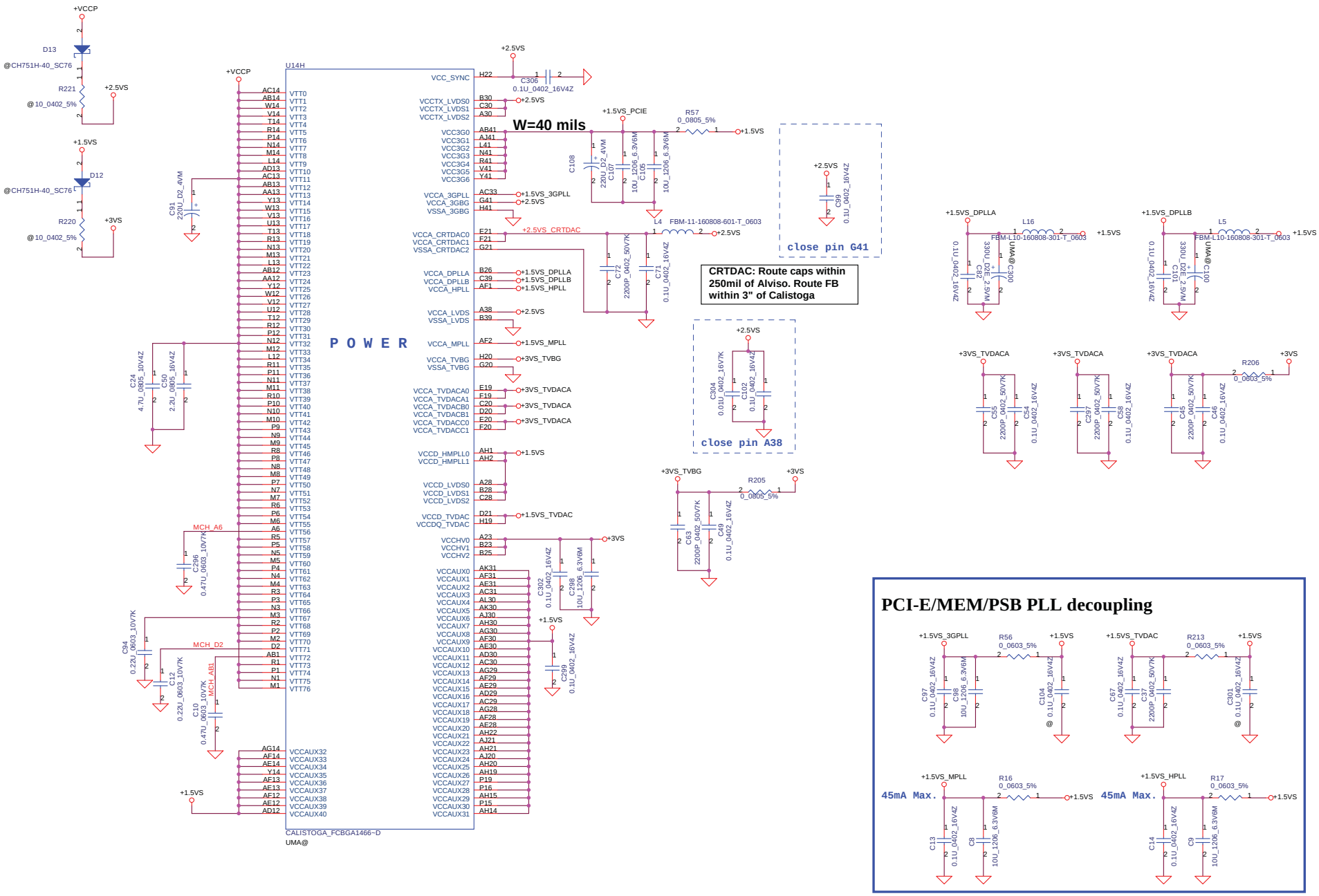

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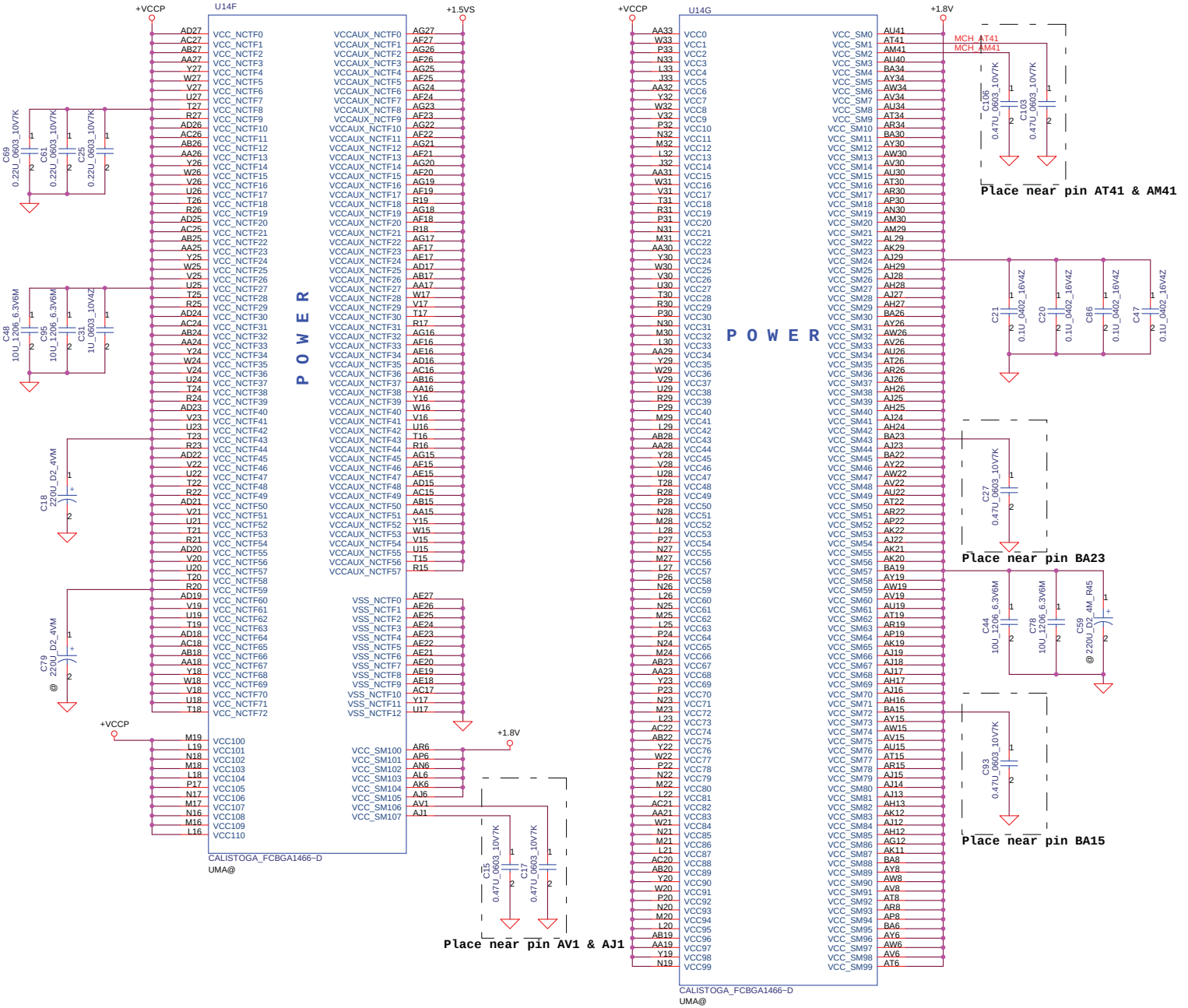
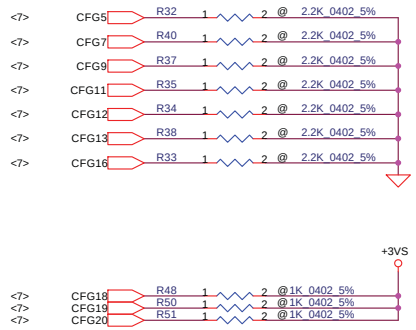


Strap Pin Table

CFG[3:17] have internal pull up

CFG[19:18] have internal pull down

CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4*(Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU*(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation (Default)*
CFG6 PSB 4X CLK Enable	0 = Reserved 1 = Calistoga *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation *(Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG10 CFG18	10 = 1.05V*(Default) 01 = 1.5V
CFG19	0 = Normal Operation * (Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present * (Default) 1 = SDVO Device Present
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. *(Default) 1 = PCIE/SDVO are operating simu.



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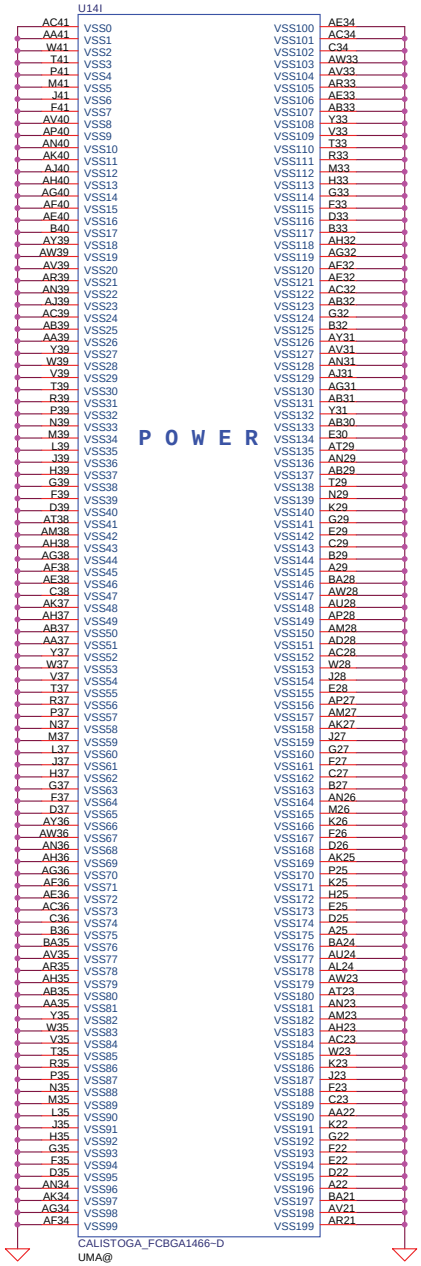

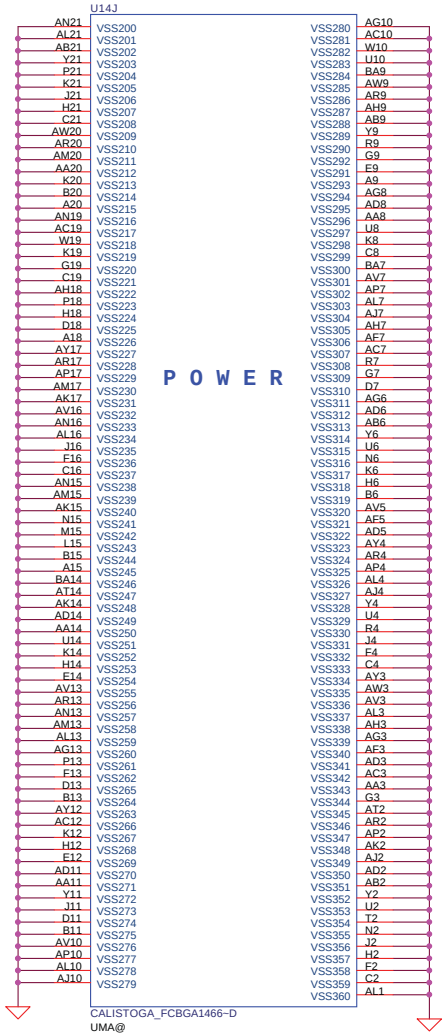

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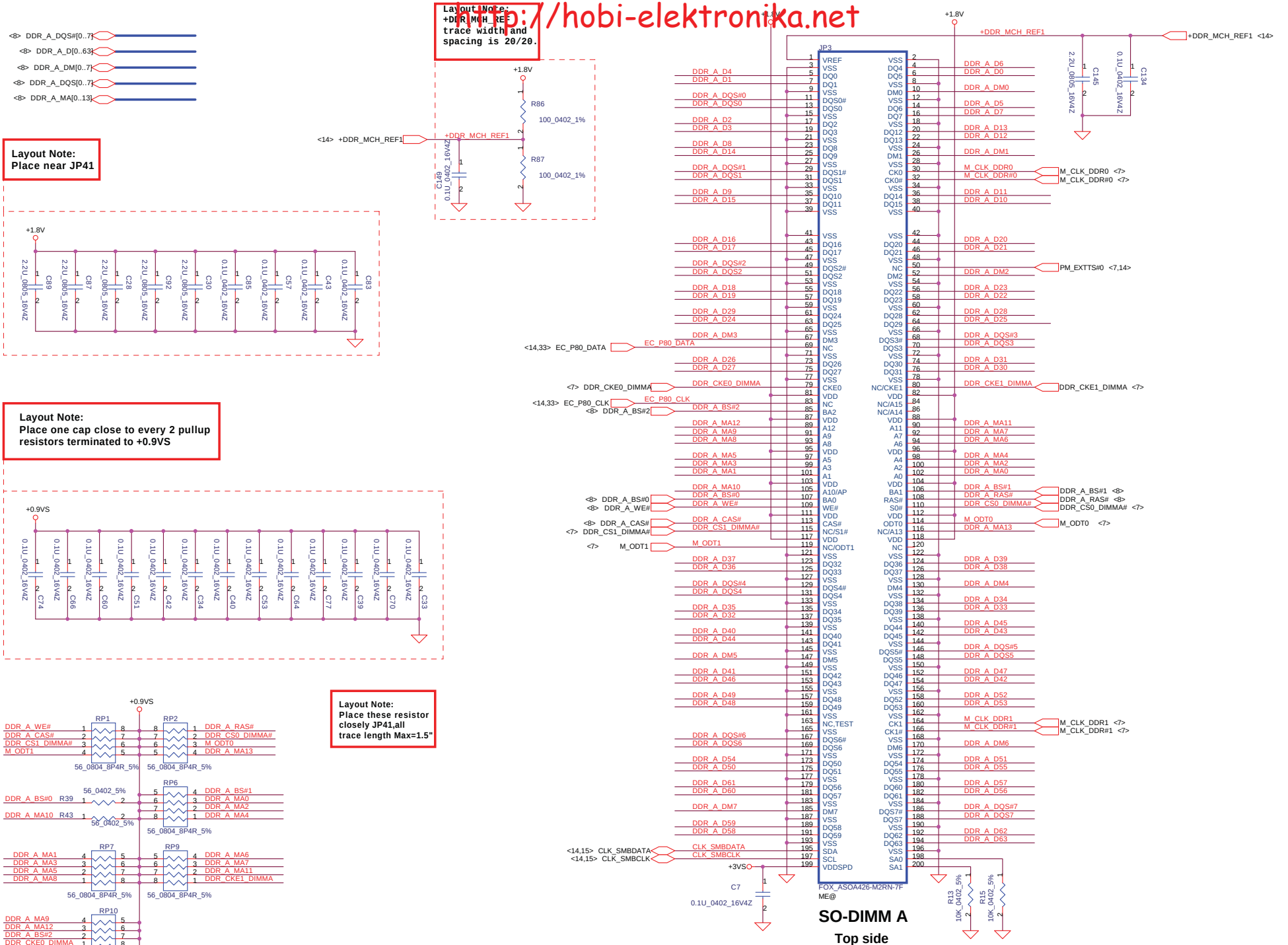

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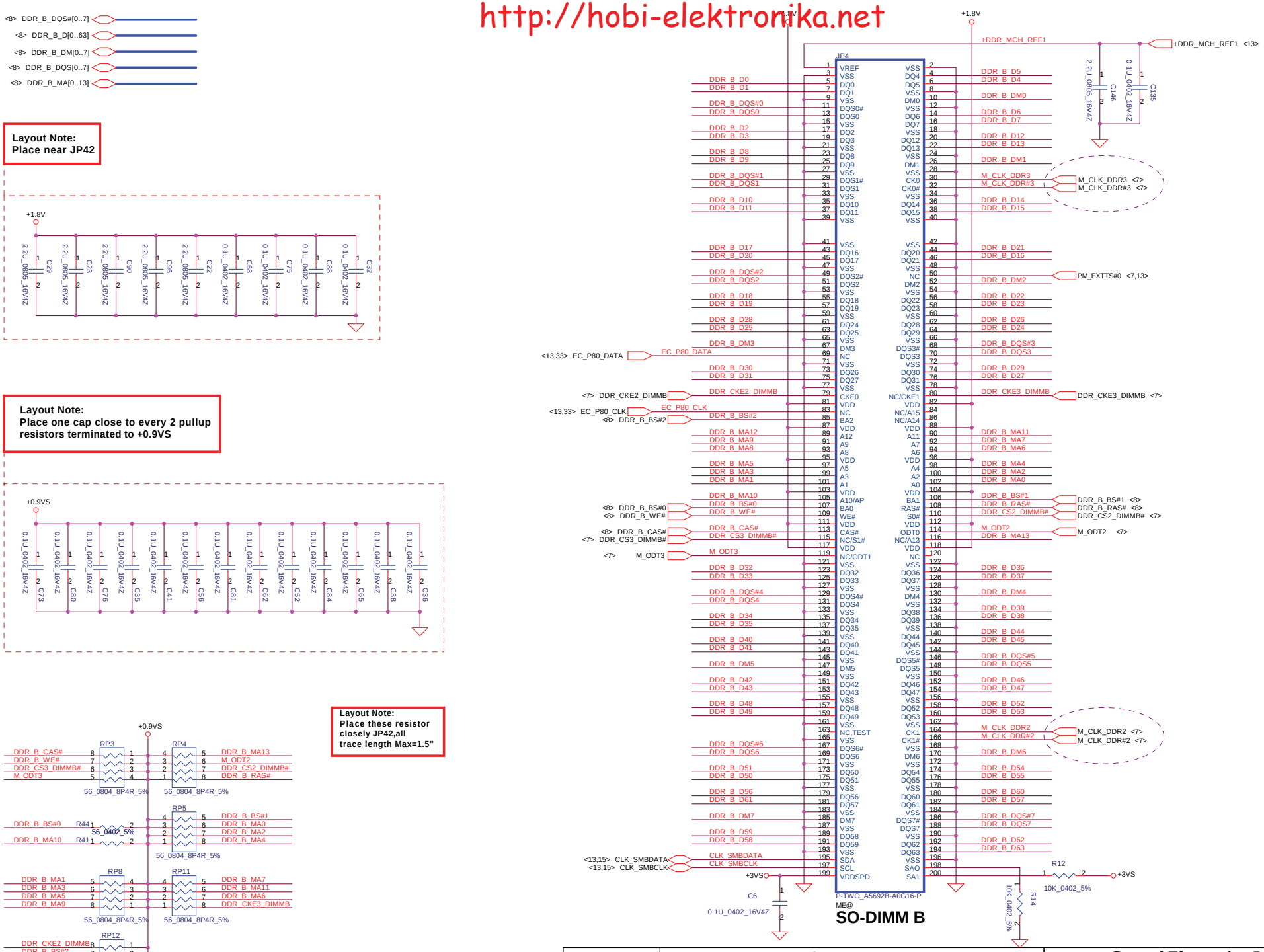

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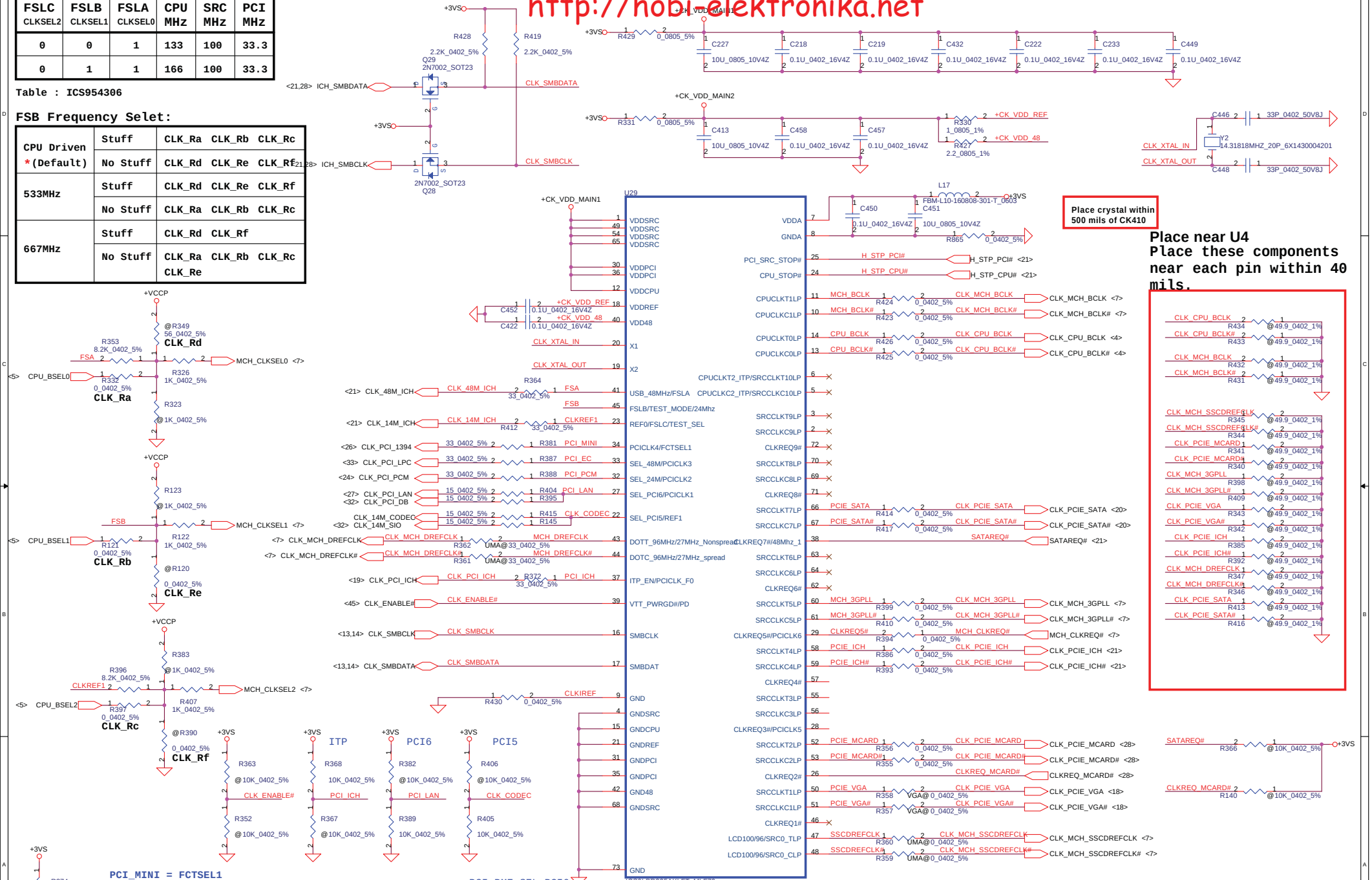
FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	1	133	100	33.3
0	1	1	166	100	33.3

Table : ICS954306

FSB Frequency Selet:

CPU Driven *(Default)	Stuff	CLK_Ra CLK_Rb CLK_Rc
	No Stuff	CLK_Rd CLK_Re CLK_Rf
533MHz	Stuff	CLK_Rd CLK_Re CLK_Rf
	No Stuff	CLK_Ra CLK_Rb CLK_Rc
667MHz	Stuff	CLK_Rd CLK_Rf
	No Stuff	CLK_Ra CLK_Rb CLK_Rc CLK_Re



FCTSEL1 (PIN34)	PIN43	PIN44	PIN47	PIN48
0	DOT96T	DOT96C	96/100M_T	96/100M_C
1	27Mout	27MSSout	SRCT0	SRCC0

PCI_LAN	PIN27
0	CLKREQ5
1	PCICLK6

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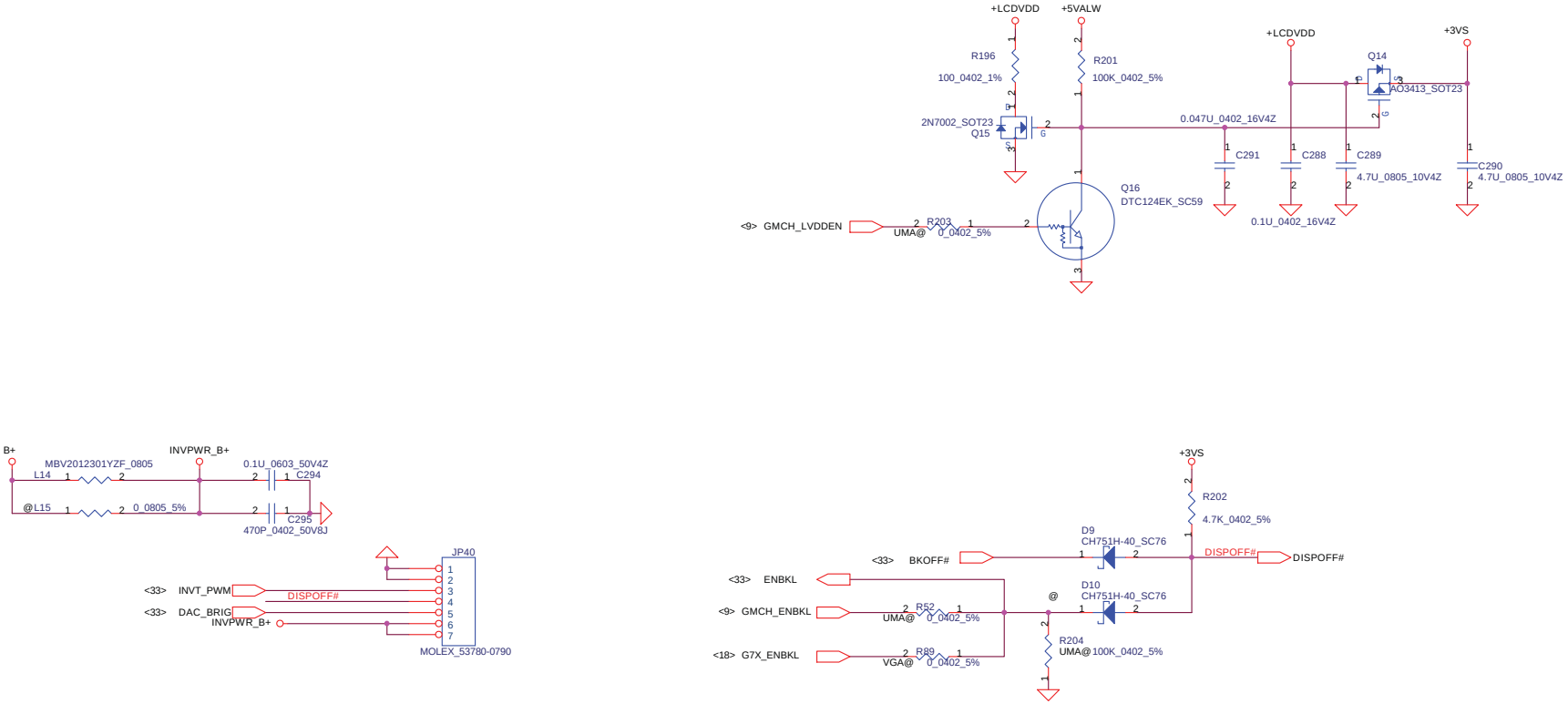

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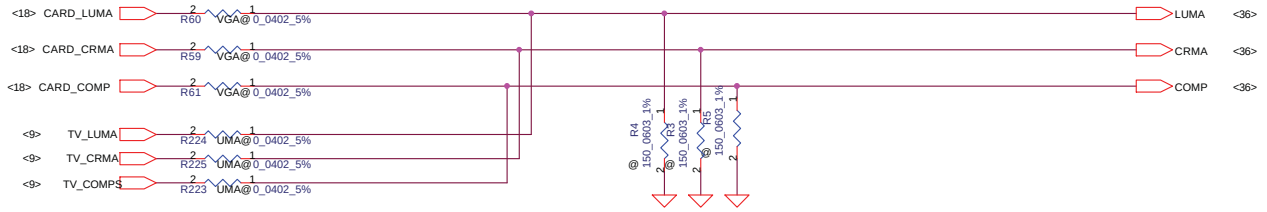
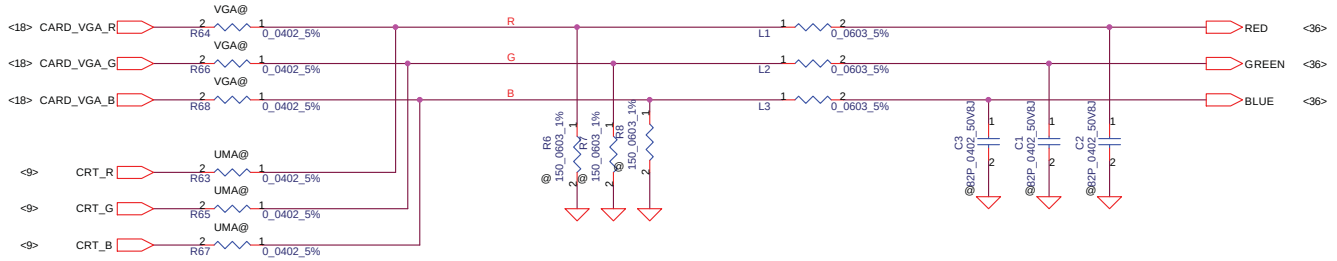
TV-OUT Conn.



Pop when with internal graphics

CRT Conn.



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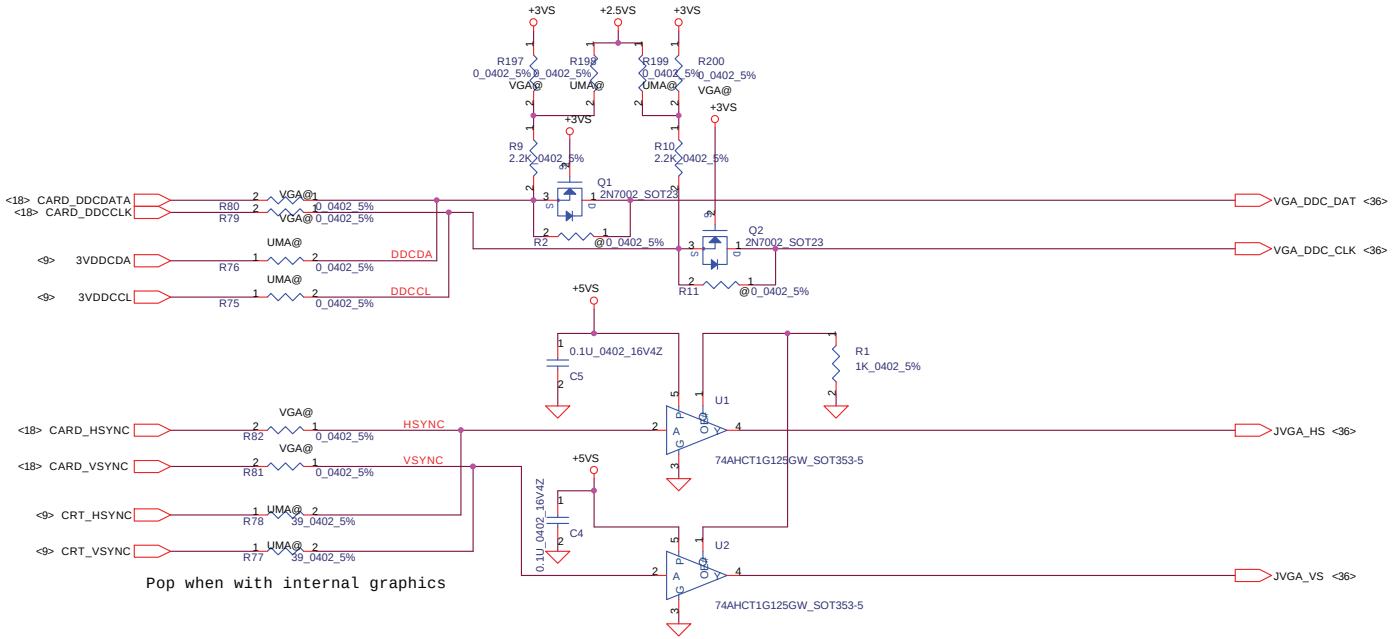

Pop when with internal graphics

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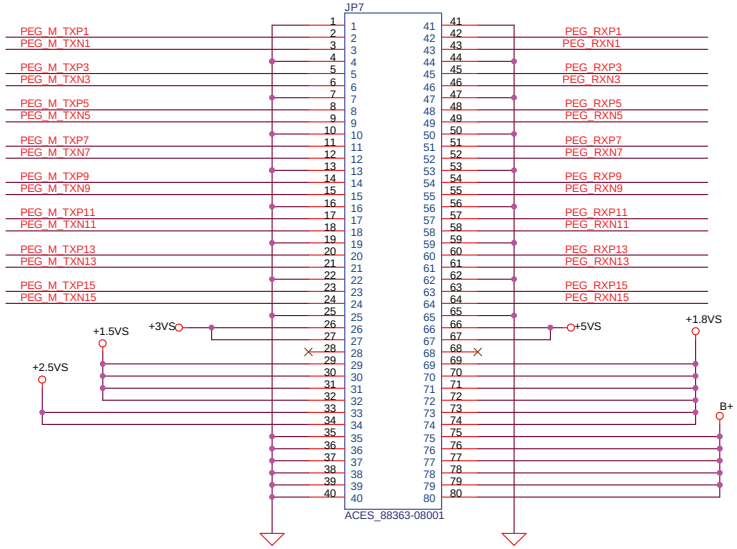
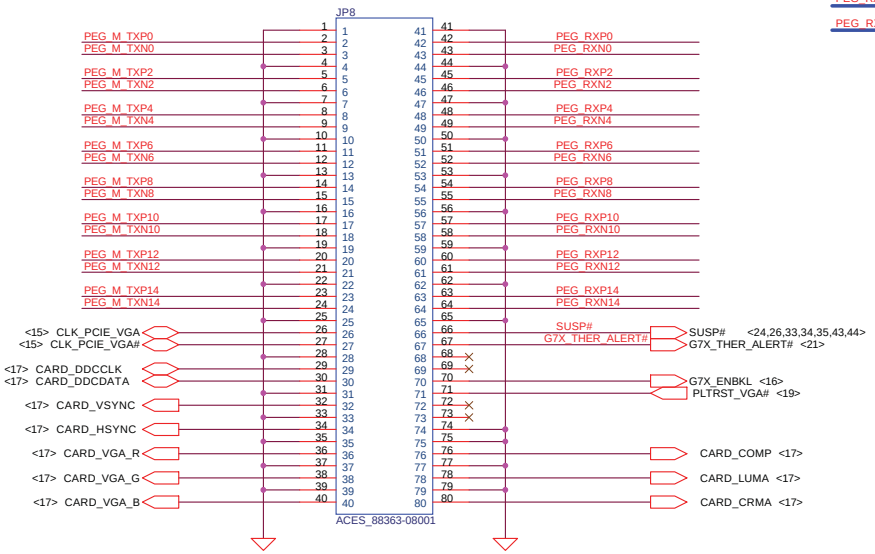
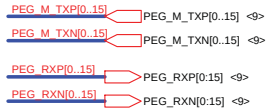
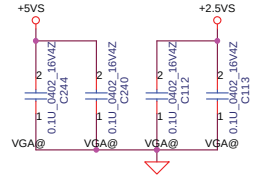
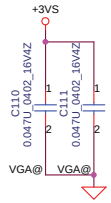
MAX. 4.06A @ 1.8V
MAX. 130mA @ 2.5V
MAX. 655mA @ 3.3V











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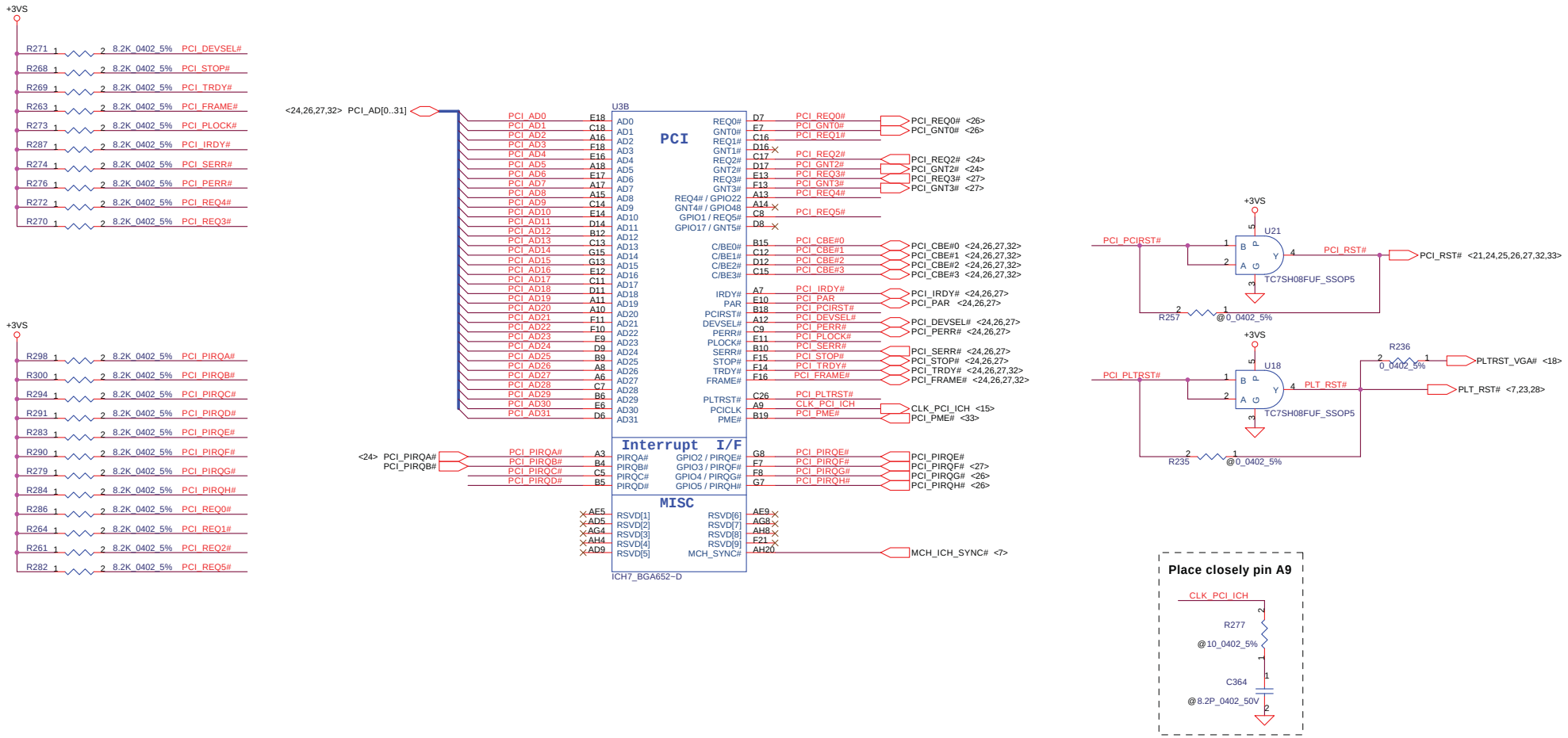

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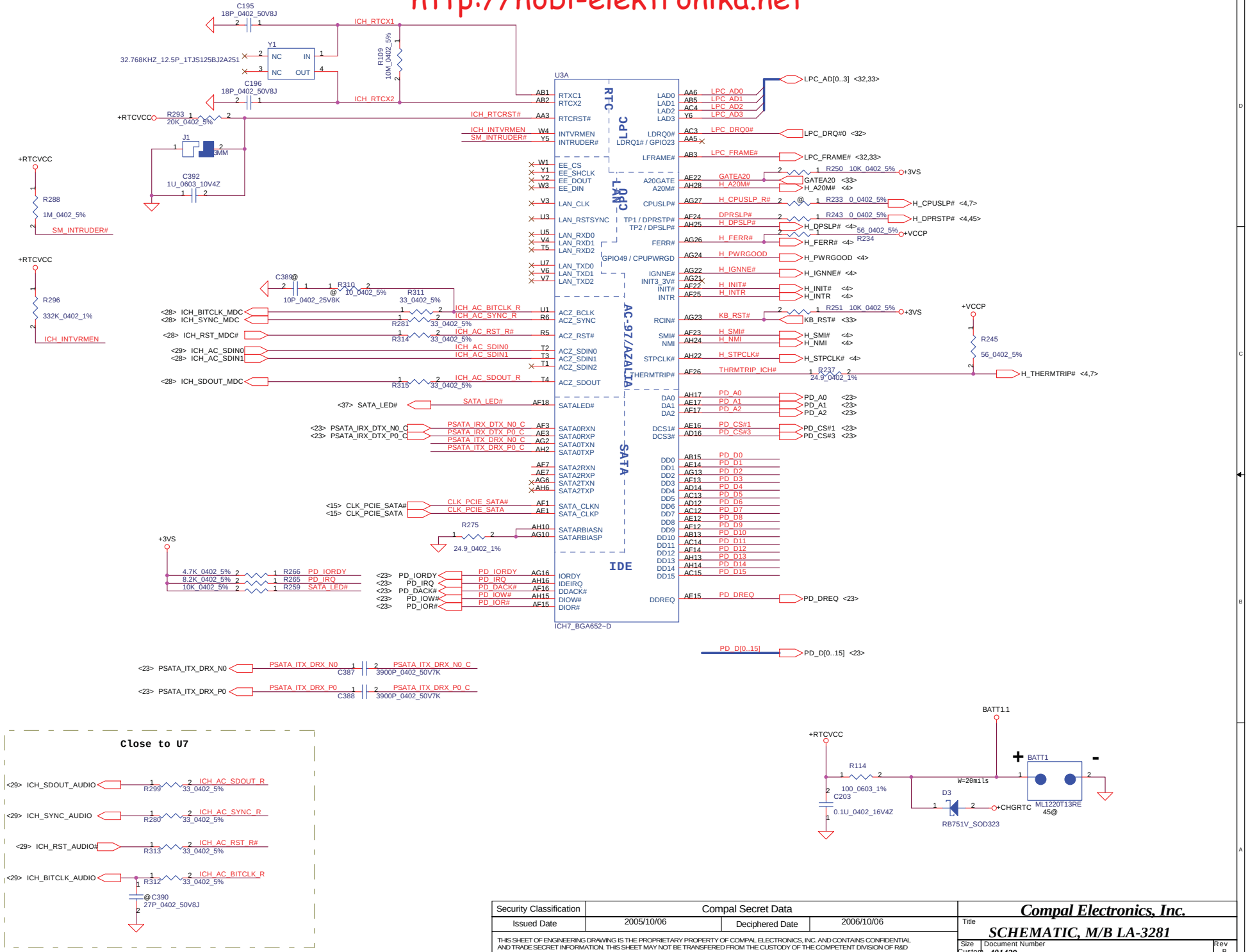

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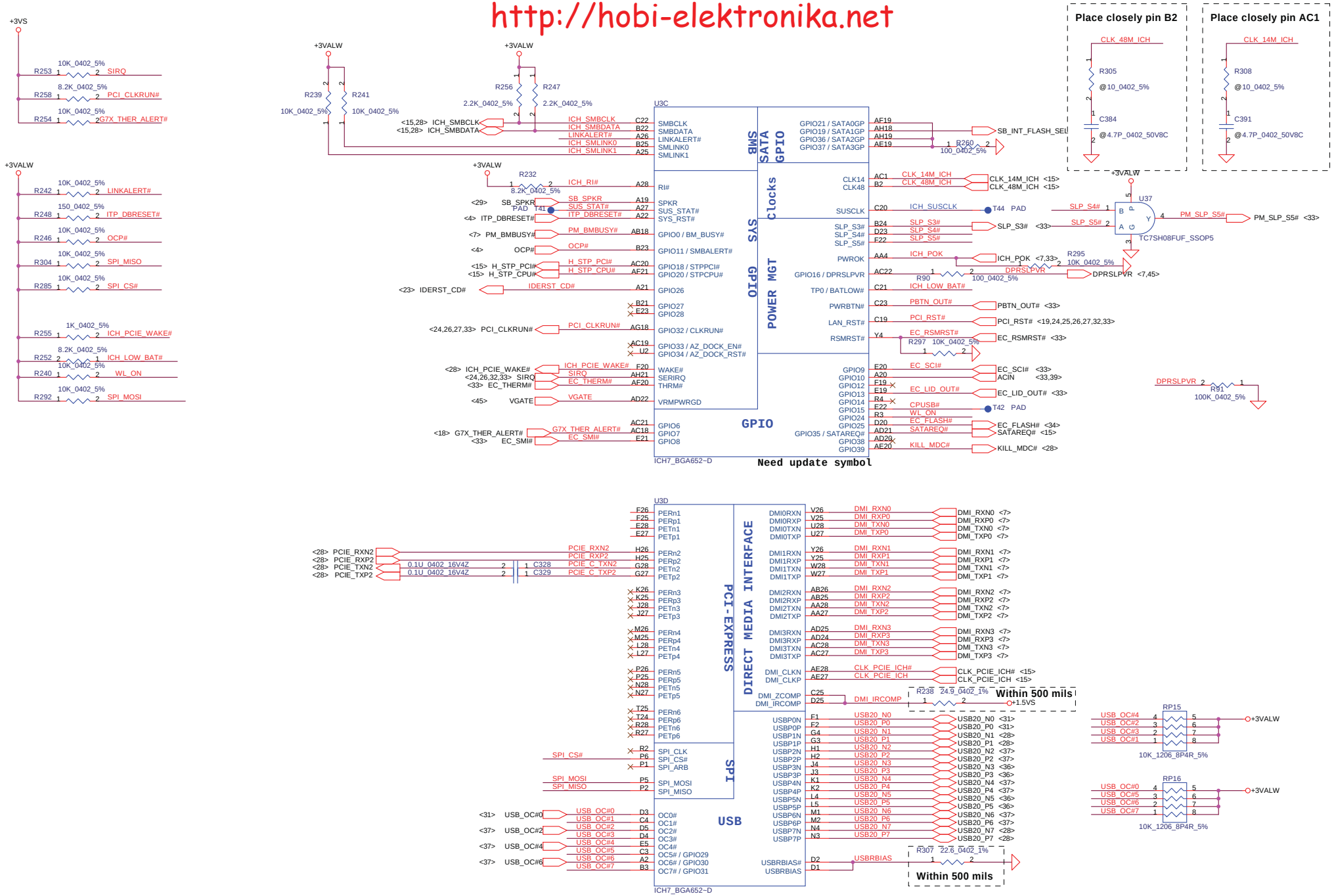

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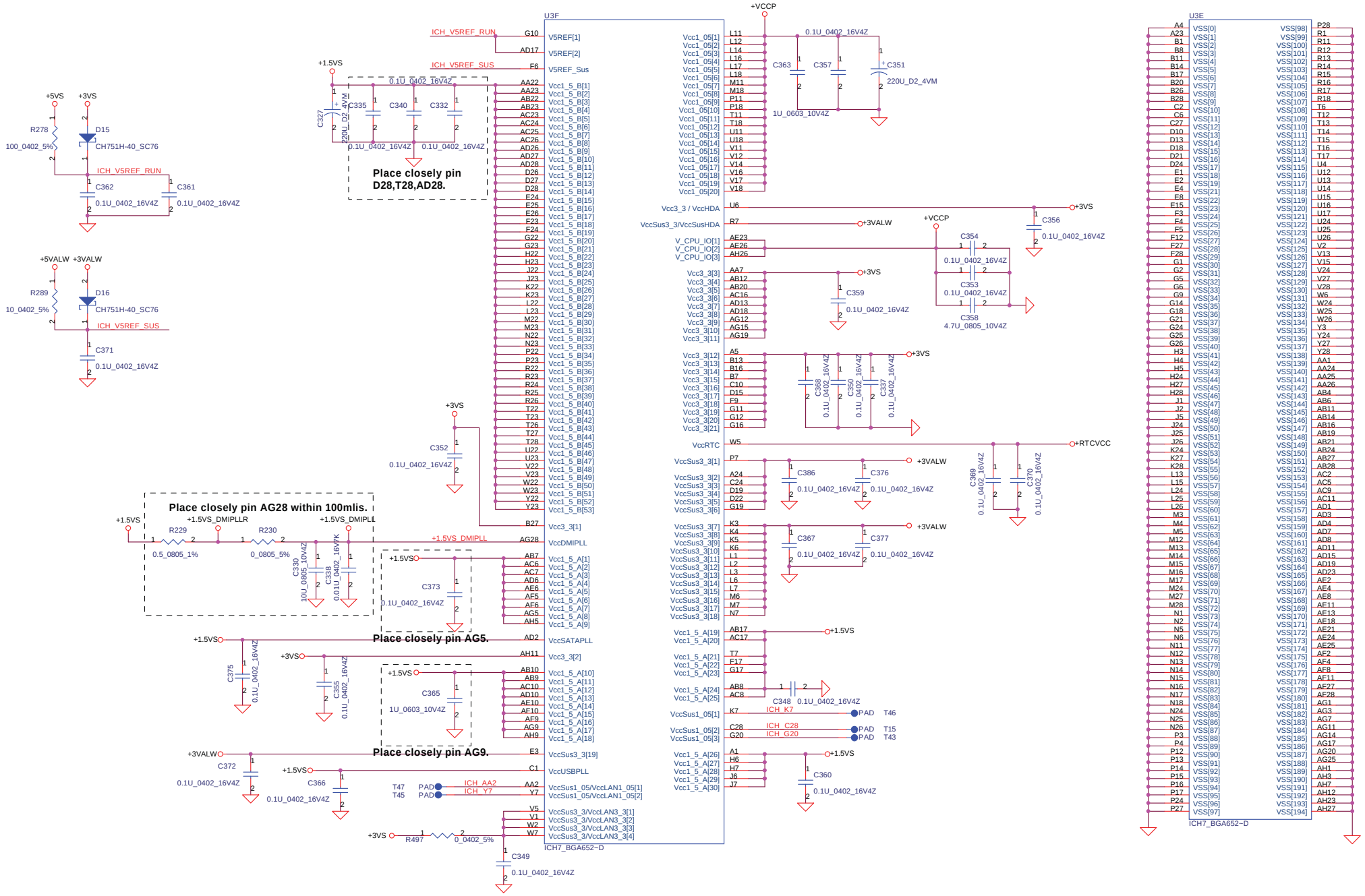

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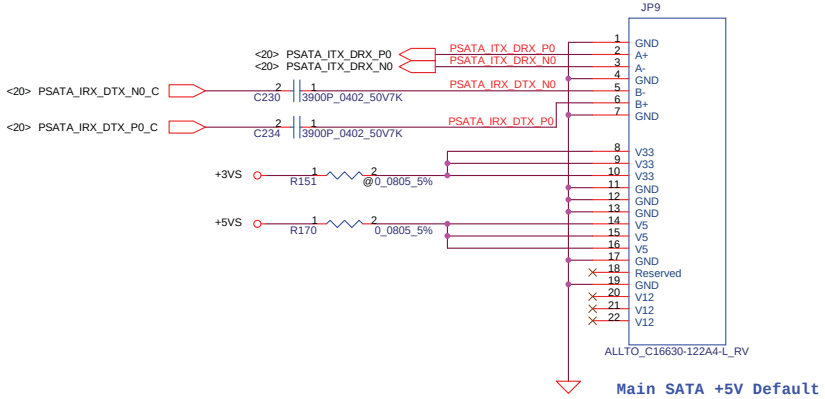

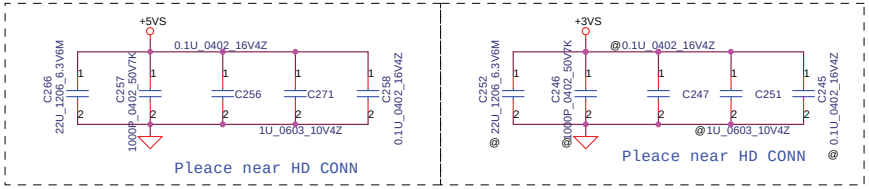

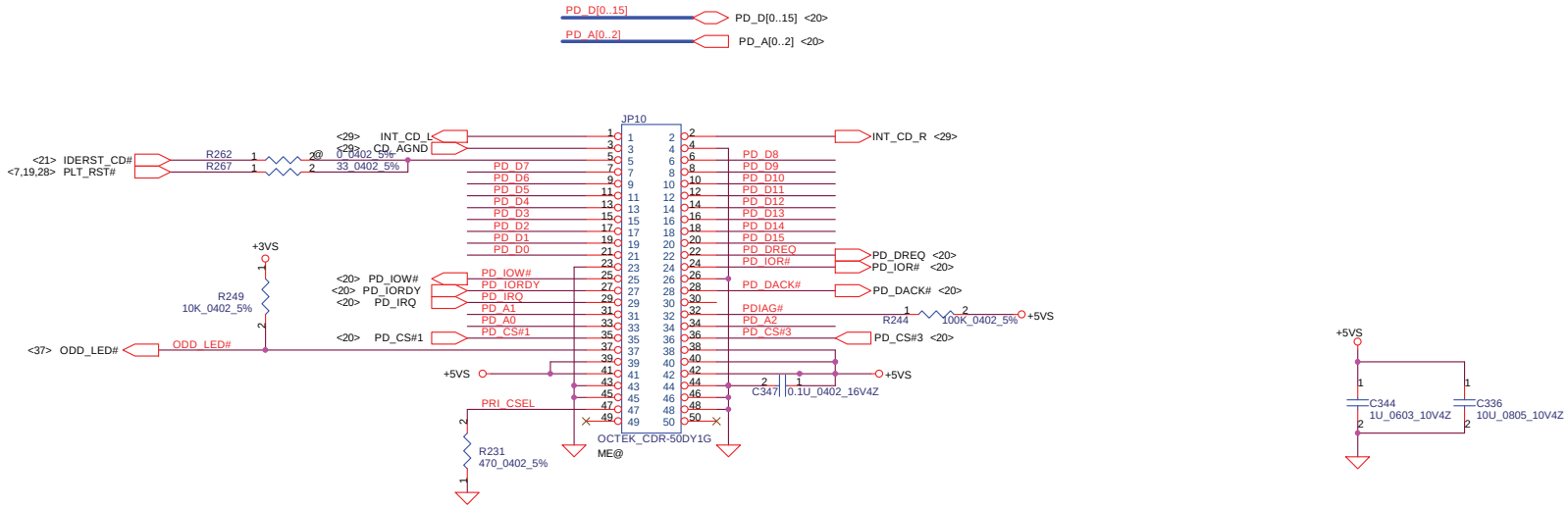

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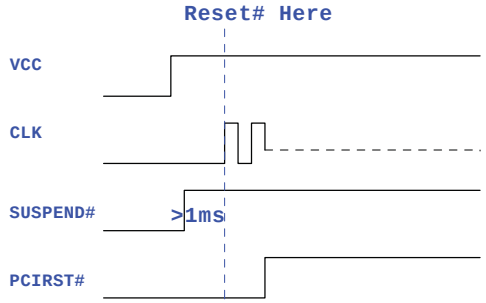
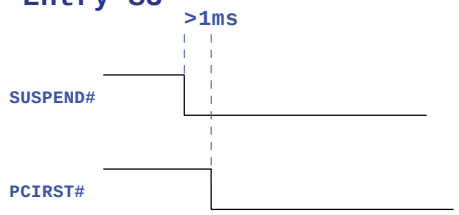
Power on RESET#



Entry S3



SUSPEND# will gate the PCIRST# or GRST#, so need S3 wake up function, SUSPEND# must be LOW ahead the PCIRST# about 1ms.

CARD_S1_A[0..25] — CARD_S1_A[0..25] <25>
CARD_S1_D[0..15] — CARD_S1_D[0..15] <25>
PCI_AD[0..31] — PCI_AD[0..31] <19,26,27,32>

+3VS, +S1_VCC

C400 4.7U_0805_10V4Z; C402 0.1U_0402_16V4Z; C456 0.1U_0402_16V4Z; C436 0.1U_0402_16V4Z; C403 0.1U_0402_16V4Z

C431 0.1U_0402_16V4Z; C438 0.1U_0402_16V4Z; C454 0.1U_0402_16V4Z; C455 0.1U_0402_16V4Z; C445 0.1U_0402_16V4Z; C404 0.1U_0402_16V4Z; C421 0.1U_0402_16V4Z

<25> VPPD0
<25> VPPD1
<25> VCCD0#
<25> VCCD1#

ENE CB1410 just have one vcc plane internal, if want S3 wake-up function(PME#),then at S3 status must keep all Vcc +3V. That is different with TI 1410 and O2-Micro 6912, just keep the VCCI pin +3V, the other vcc can use +3VS.

U28 — PQFP 144, 22.2 X 22.2 X 1.60 — CB1410_LQFP144

Pin	Signal	Net
3	AD31	PCI_AD31
4	AD30	PCI_AD30
5	AD29	PCI_AD29
7	AD28	PCI_AD28
8	AD27	PCI_AD27
9	AD26	PCI_AD26
10	AD25	PCI_AD25
11	AD24	PCI_AD24
15	AD23	PCI_AD23
16	AD22	PCI_AD22
17	AD21	PCI_AD21
19	AD20	PCI_AD20
23	AD19	PCI_AD19
24	AD18	PCI_AD18
25	AD17	PCI_AD17
26	AD16	PCI_AD16
38	AD15	PCI_AD15
39	AD14	PCI_AD14
40	AD13	PCI_AD13
41	AD12	PCI_AD12
43	AD11	PCI_AD11
45	AD10	PCI_AD10
46	AD9	PCI_AD9
47	AD8	PCI_AD8
49	AD7	PCI_AD7
51	AD6	PCI_AD6
52	AD5	PCI_AD5
53	AD4	PCI_AD4
54	AD3	PCI_AD3
55	AD2	PCI_AD2
56	AD1	PCI_AD1
57	AD0	PCI_AD0
12	C/BE3#	PCI_CBE#3
27	C/BE2#	PCI_CBE#2
37	C/BE1#	PCI_CBE#1
48	C/BE0#	PCI_CBE#0
20	RST#	PCI_RST#
28	FRAME#	PCI_FRAME#
29	IRDY#	PCI_IRDY#
31	TRDY#	PCI_TRDY#
32	DEVSEL#	PCI_DEVSEL#
33	STOP#	PCI_STOP#
34	PERR#	PCI_PERR#
35	SERR#	PCI_SERR#
36	PAR	PCI_PAR
1	REQ#	PCI_REQ2#
2	GNT#	PCI_GNT2#
21	PCLK	CLK_PCI_PCM
59	RI_OUT#/PME#	CB_PME#
70	SUSPEND#	SUSP#
13	IDSEL	PCI_AD20
60	MFUNC0	PCI_PIRQA#
61	MFUNC1	
64	MFUNC2	
65	MFUNC3	SIRQ
67	MFUNC4	
68	MFUNC5	
69	MFUNC6	PCI_CLKRUN#
66	VCC/GRST#	PCI_RST#
144	CAD31/D10	CARD_S1_D10
142	CAD30/D9	CARD_S1_D9
141	CAD29/D1	CARD_S1_D1
140	CAD28/D8	CARD_S1_D8
139	CAD27/D0	CARD_S1_D0
129	CAD26/A0	CARD_S1_A0
128	CAD25/A1	CARD_S1_A1
127	CAD24/A2	CARD_S1_A2
124	CAD23/A3	CARD_S1_A3
121	CAD22/A4	CARD_S1_A4
120	CAD21/A5	CARD_S1_A5
118	CAD20/A6	CARD_S1_A6
116	CAD19/A25	CARD_S1_A25
115	CAD18/A7	CARD_S1_A7
113	CAD17/A24	CARD_S1_A24
98	CAD16/A17	CARD_S1_A17
96	CAD15/IOWR#	CARD_S1_IOWR# — CARD_S1_IOWR# <25>
97	CAD14/A9	CARD_S1_A9
93	CAD13/IORD#	CARD_S1_IORD# — CARD_S1_IORD# <25>
95	CAD12/A11	CARD_S1_A11
92	CAD11/OE#	CARD_S1_OE# — CARD_S1_OE# <25>
91	CAD10/CE2#	CARD_S1_CE2# — CARD_S1_CE2# <25>
89	CAD9/A10	CARD_S1_A10
87	CAD8/D15	CARD_S1_D15
85	CAD7/D7	CARD_S1_D7
82	CAD6/D13	CARD_S1_D13
83	CAD5/D6	CARD_S1_D6
80	CAD4/D12	CARD_S1_D12
81	CAD3/D5	CARD_S1_D5
77	CAD2/D11	CARD_S1_D11
79	CAD1/D4	CARD_S1_D4
76	CAD0/D3	CARD_S1_D3
125	CC/BE3#/REG#	CARD_S1_REG# — CARD_S1_REG# <25>
112	CC/BE2#/A12	CARD_S1_A12
99	CC/BE1#/A8	CARD_S1_A8
88	CC/BE0#/CE1#	CARD_S1_CE1# — CARD_S1_CE1# <25>
119	CRST#/RESET	CARD_S1_RST — CARD_S1_RST <25>
111	CFRAME#/A23	CARD_S1_A23
110	CIRDY#/A15	CARD_S1_A15
109	CTRDY#/A22	CARD_S1_A22
107	CDEVSEL#/A21	CARD_S1_A21
105	CSTOP#/A20	CARD_S1_A20
104	CPERR#/A14	CARD_S1_A14
133	CSERR#/WAIT#	CARD_S1_WAIT# — CARD_S1_WAIT# <25>
101	CPAR/A13	CARD_S1_A13
123	CREQ#/INPACK#	CARD_S1_INPACK# — CARD_S1_INPACK# <25>
106	CGNT#/WE#	CARD_S1_WE# — CARD_S1_WE# <25>
108	CCLK/A16	CARD_S1_A16_CLK — R420 33_0402_5% — CARD_S1_A16
135	CSTSCHG/BVD1	CARD_S1_BVD1 — CARD_S1_BVD1 <25>
136	CCLKRUN#/WP	CARD_S1_WP — CARD_S1_WP <25>
103	CBLOCK#/A19	CARD_S1_A19
132	CINT#/READY	CARD_S1_RDY# — CARD_S1_RDY# <25>
62	SPKOUT	PCM_SPK# — PCM_SPK# <29>
134	CAUDIO/BVD2	CARD_S1_BVD2 — CARD_S1_BVD2 <25>
137	CCD2#/CD2#	CARD_S1_CD2# — CARD_S1_CD2# <25>
75	CCD1#/CD1#	CARD_S1_CD1# — CARD_S1_CD1# <25>
117	CVS2/VS2#	CARD_S1_VS2 — CARD_S1_VS2 <25>
131	CVS1/VS1#	CARD_S1_VS1 — CARD_S1_VS1 <25>
6, 22, 42, 58, 78, 94, 114, 130	GND1–GND8	
84, 100, 143	RSVD/D14, RSVD/A18, RSVD/D2	CARD_S1_D2, CARD_S1_A18, CARD_S1_D14

CARD_S1_OE# — R806 — 2@43K_0402_5%
CARD_S1_CE2# — R807 — 2@43K_0402_5%
CARD_S1_CE1# — R808 — 2@43K_0402_5%
CARD_S1_RST — R809 — 2@43K_0402_5%

+3VS — R318 10K_0402_5%

CLK_PCI_PCM — R379 33_0402_5%@ — C429 10P_0402_25V8K@

D17 @RB751V_SOD323 — R408 100_0402_5%

Note: MF0 -- MF6 must refer the data sheet for design.

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PROPRIETARY NOTE

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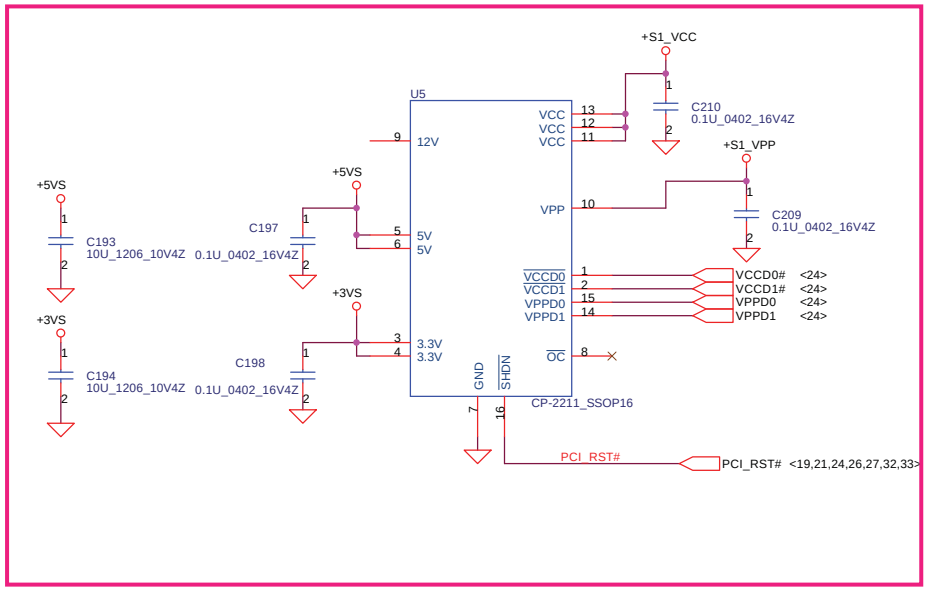
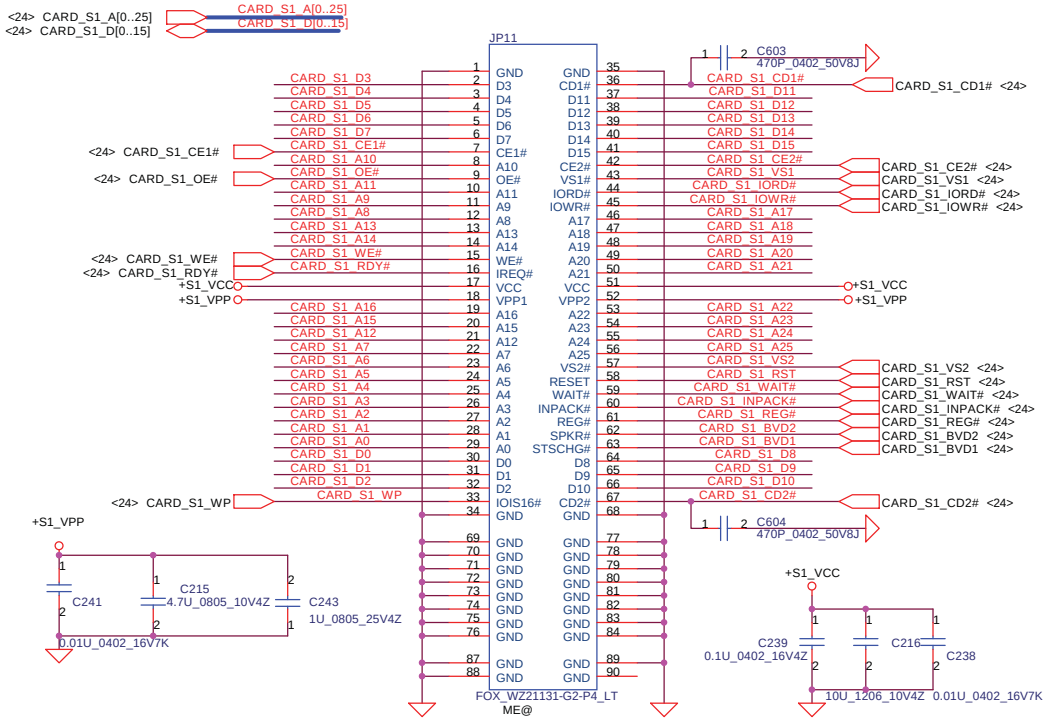
PCMCIA Power Controller





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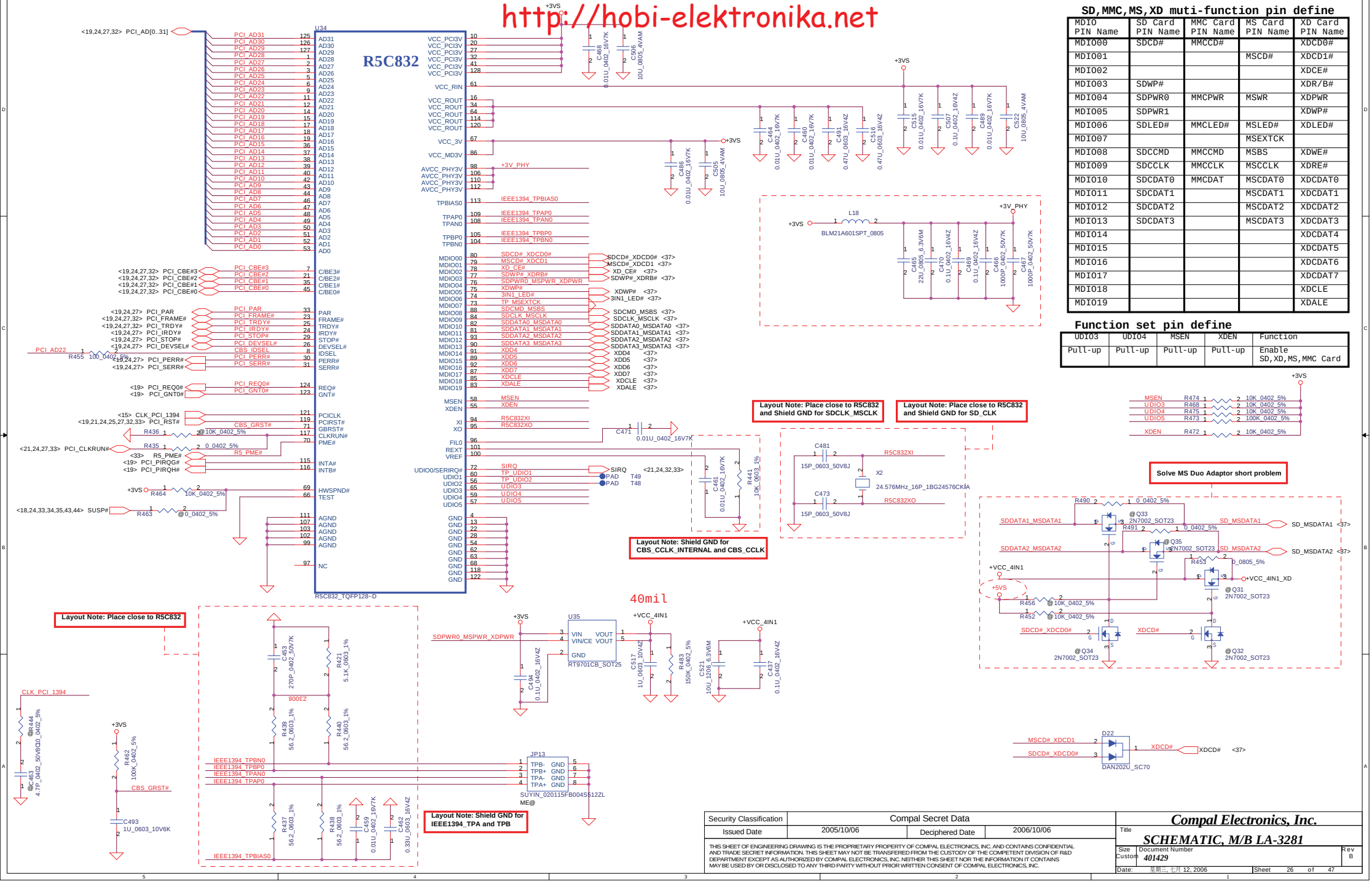

SD,MMC,MS,XD muti-function pin define

MDIO PIN Name	SD Card PIN Name	MMC Card PIN Name	MS Card PIN Name	XD Card PIN Name
MDIO00	SDCD#	MMCCD#		XDCD0#
MDIO01			MSCD#	XDCD1#
MDIO02				XDCE#
MDIO03	SDWP#			XDR/B#
MDIO04	SDPWR0	MMCPWR	MSWR	XDPWR
MDIO05	SDPWR1			XDWP#
MDIO06	SDLED#	MMCLED#	MSLED#	XDLED#
MDIO07			MSEXTCK	
MDIO08	SDCCMD	MMCCMD	MSBS	XDWE#
MDIO09	SDCCLK	MMCCLK	MSCCLK	XDRE#
MDIO10	SDCDAT0	MMCDAT	MSCDAT0	XDCDAT0
MDIO11	SDCDAT1		MSCDAT1	XDCDAT1
MDIO12	SDCDAT2		MSCDAT2	XDCDAT2
MDIO13	SDCDAT3		MSCDAT3	XDCDAT3
MDIO14				XDCDAT4
MDIO15				XDCDAT5
MDIO16				XDCDAT6
MDIO17				XDCDAT7
MDIO18				XDCLE
MDIO19				XDALE

Function set pin define

UDIO3	UDIO4	MSEN	XDEN	Function
Pull-up	Pull-up	Pull-up	Pull-up	Enable SD,XD,MS,MMC Card

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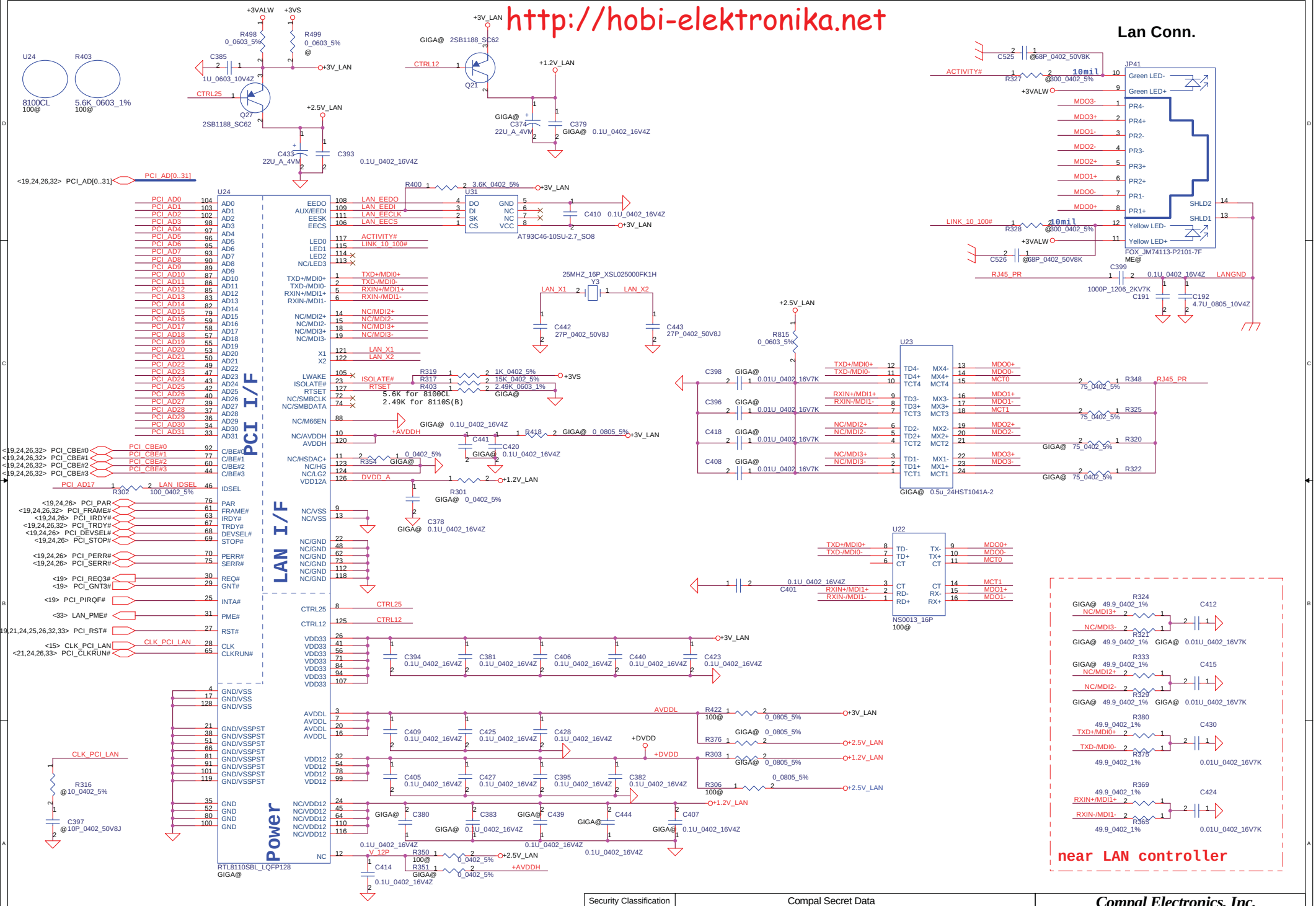
Lan Conn.



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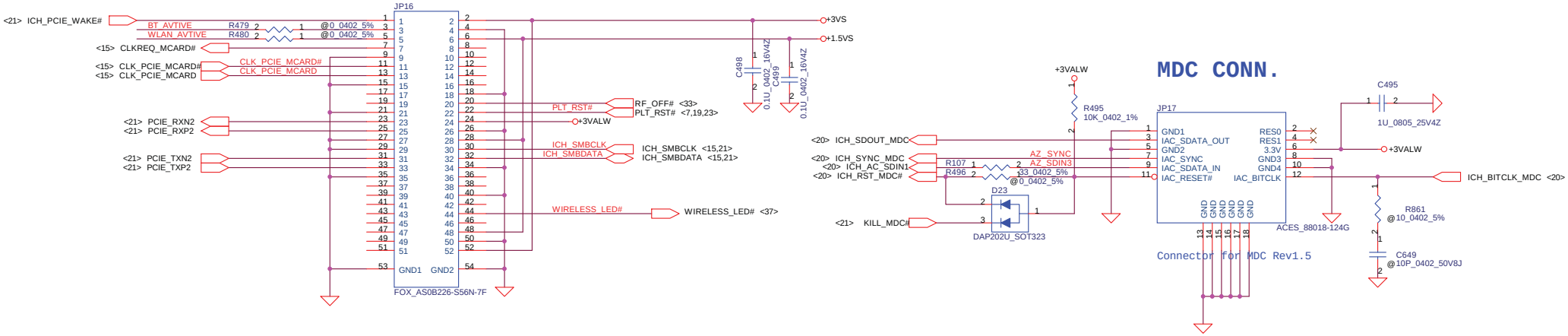
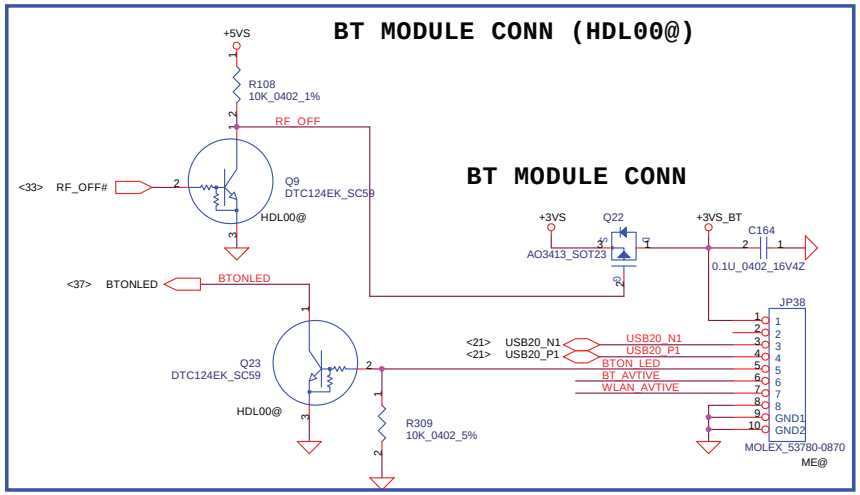
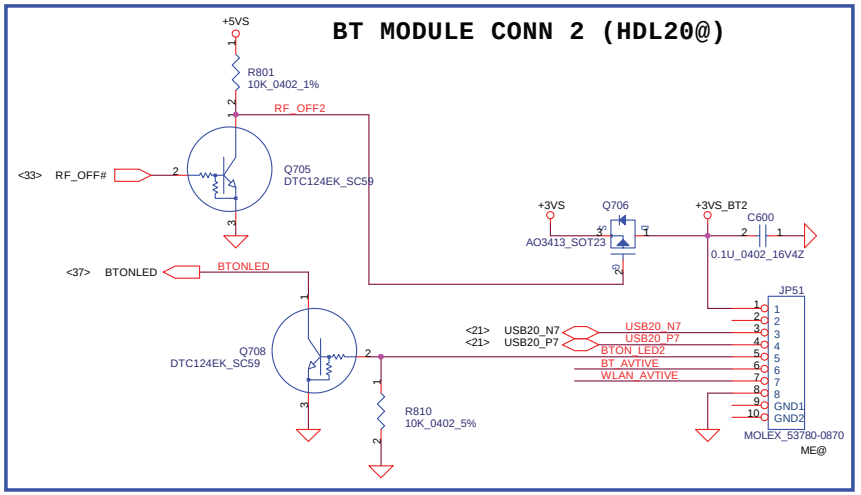
Mini-Express Card(Slot 1-WLAN)







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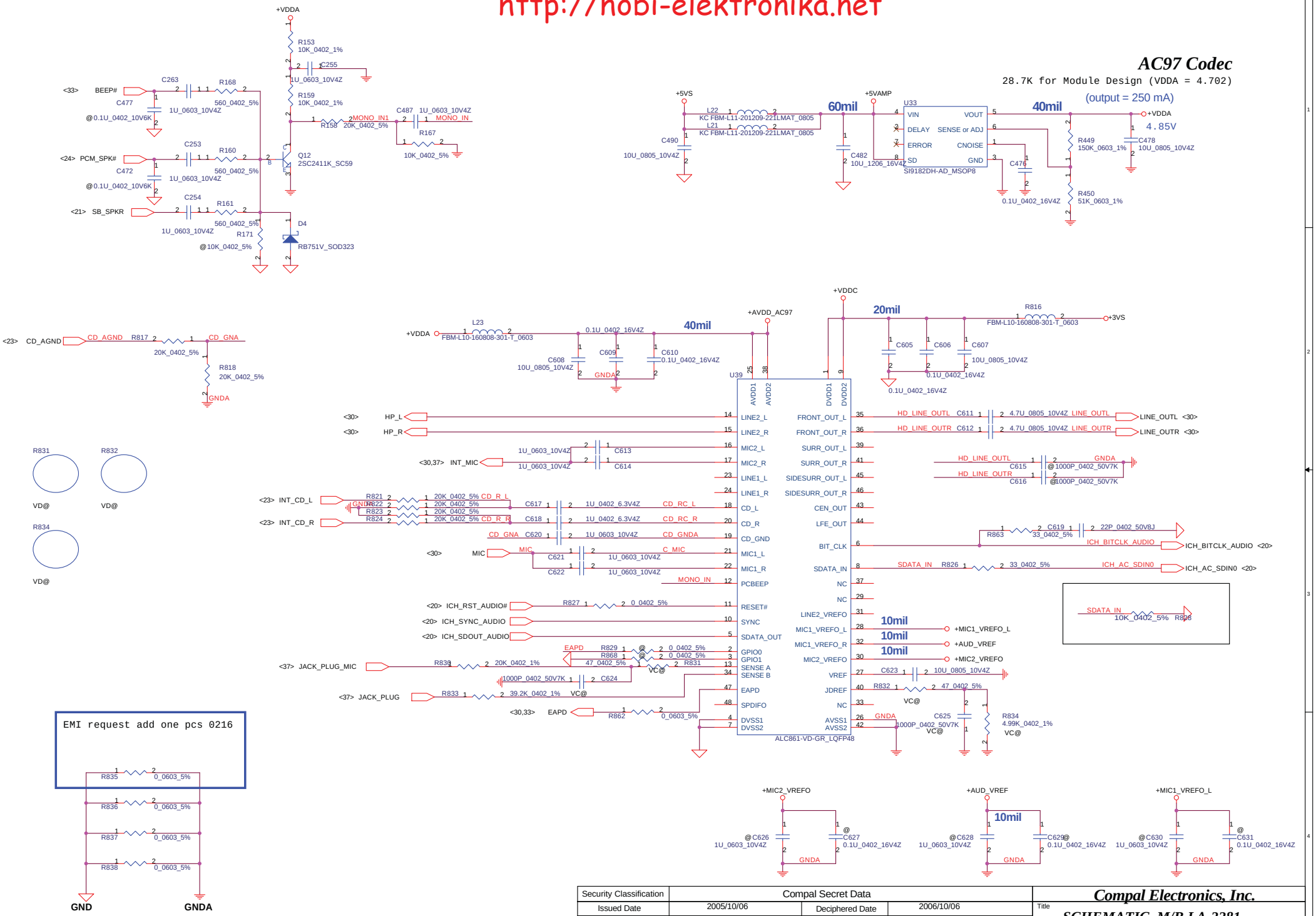
AC97 Codec

28.7K for Module Design (VDDA = 4.702)



EMI request add one pcs 0216

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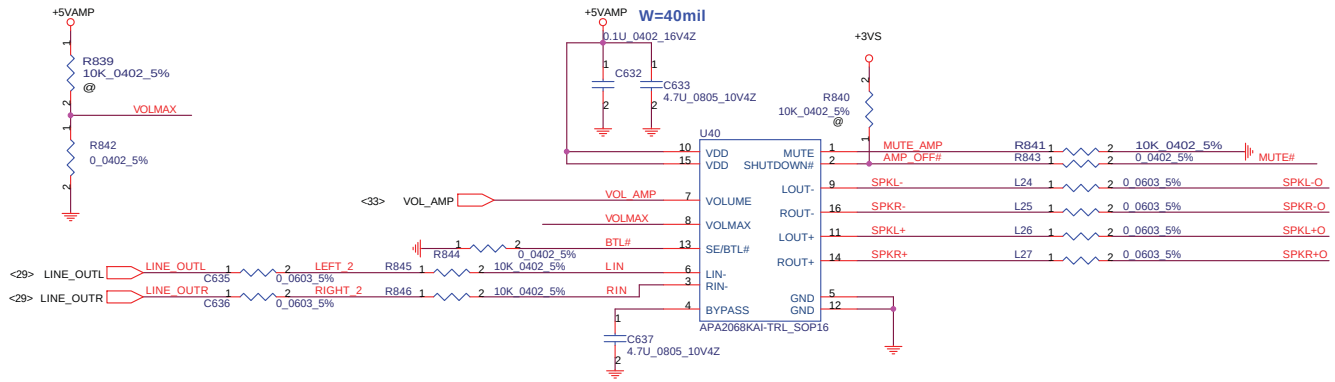

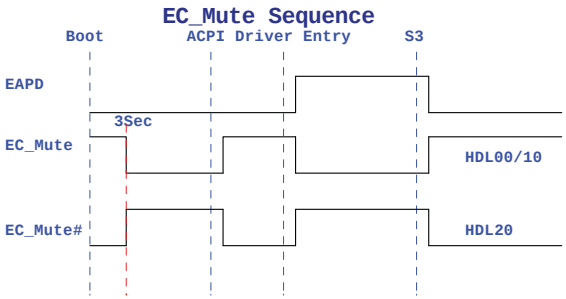

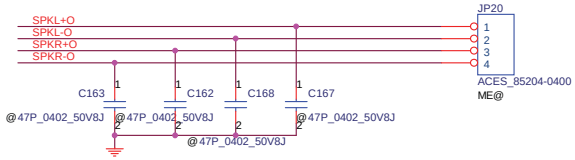

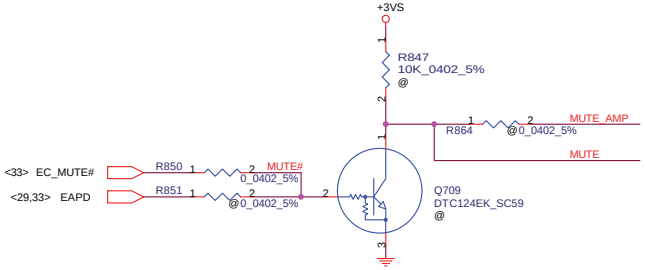

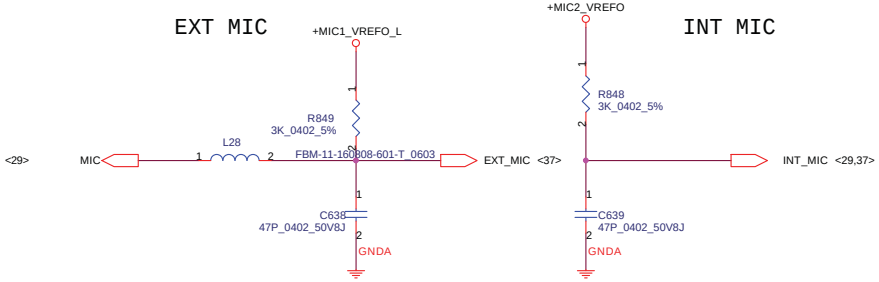

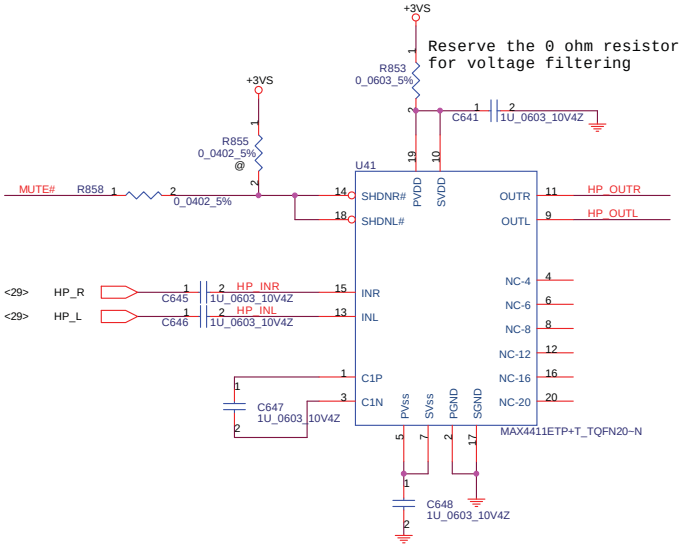

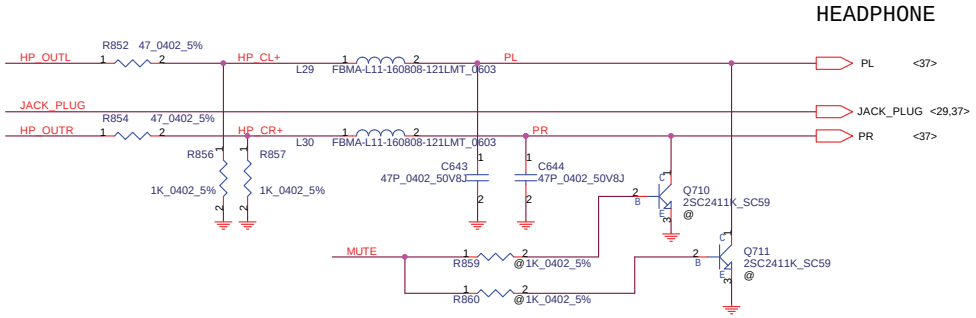

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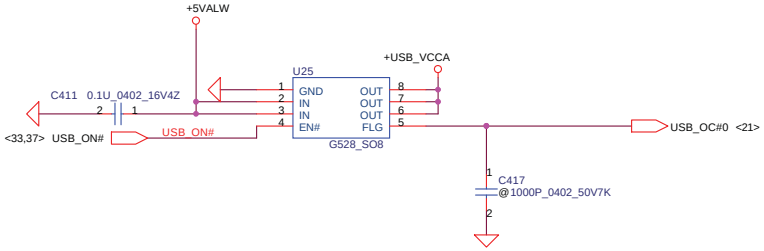

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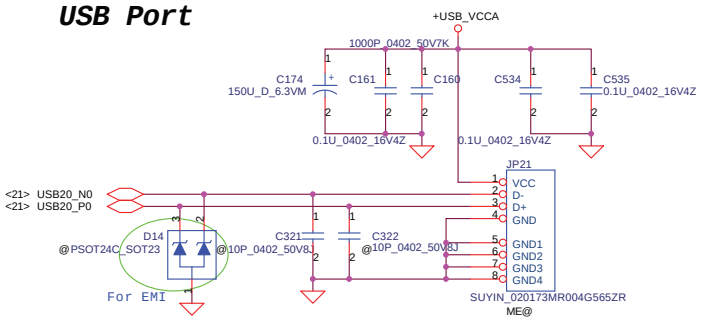

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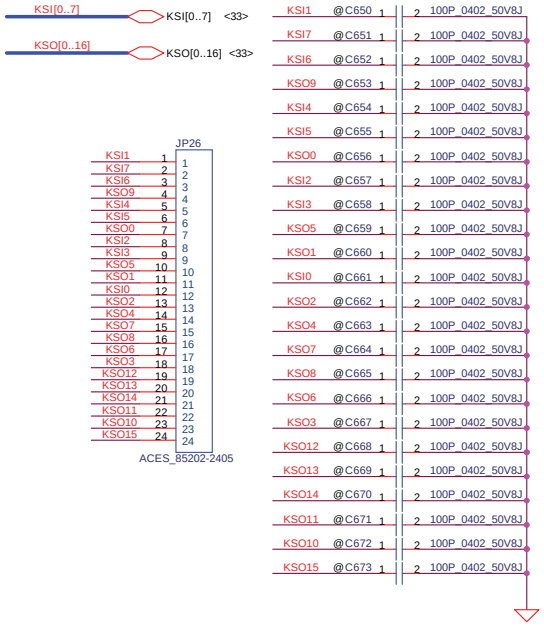
INT_KBD CONN.(TYPE "D" KB)



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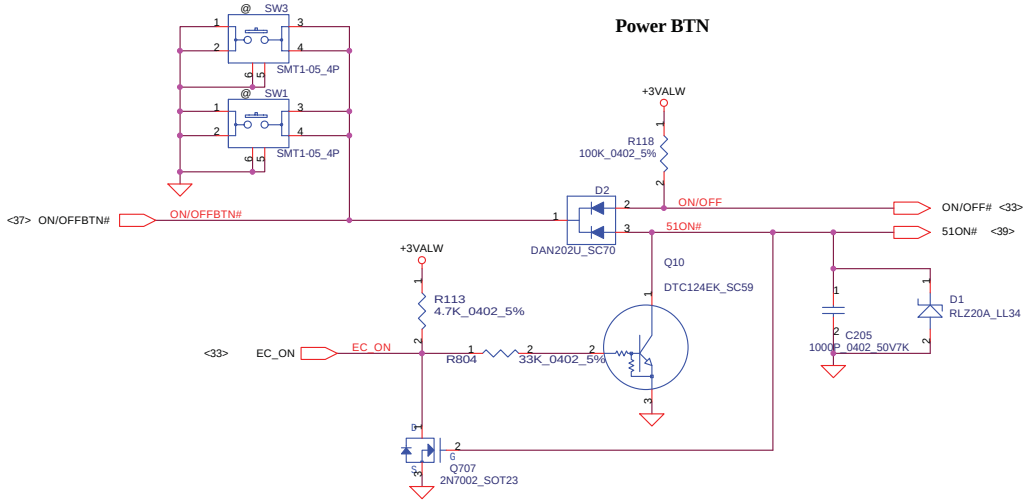

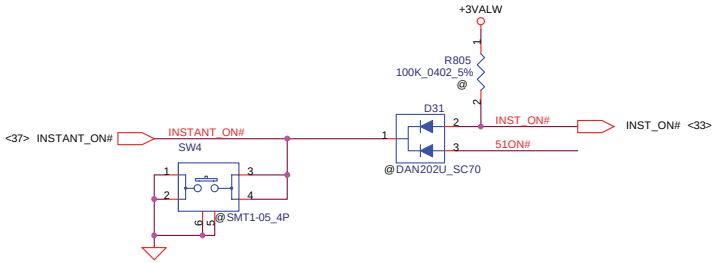

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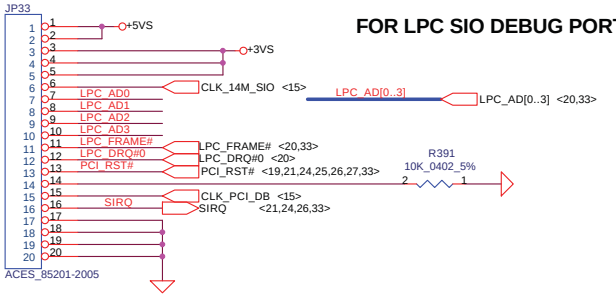

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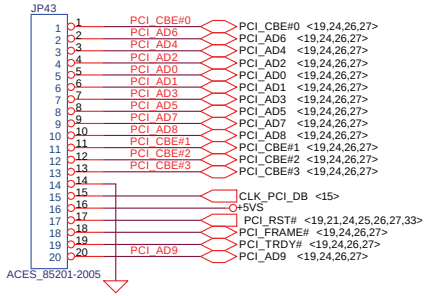
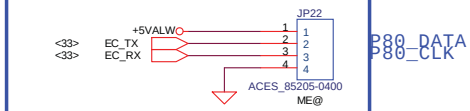


EC DEBUG PORT



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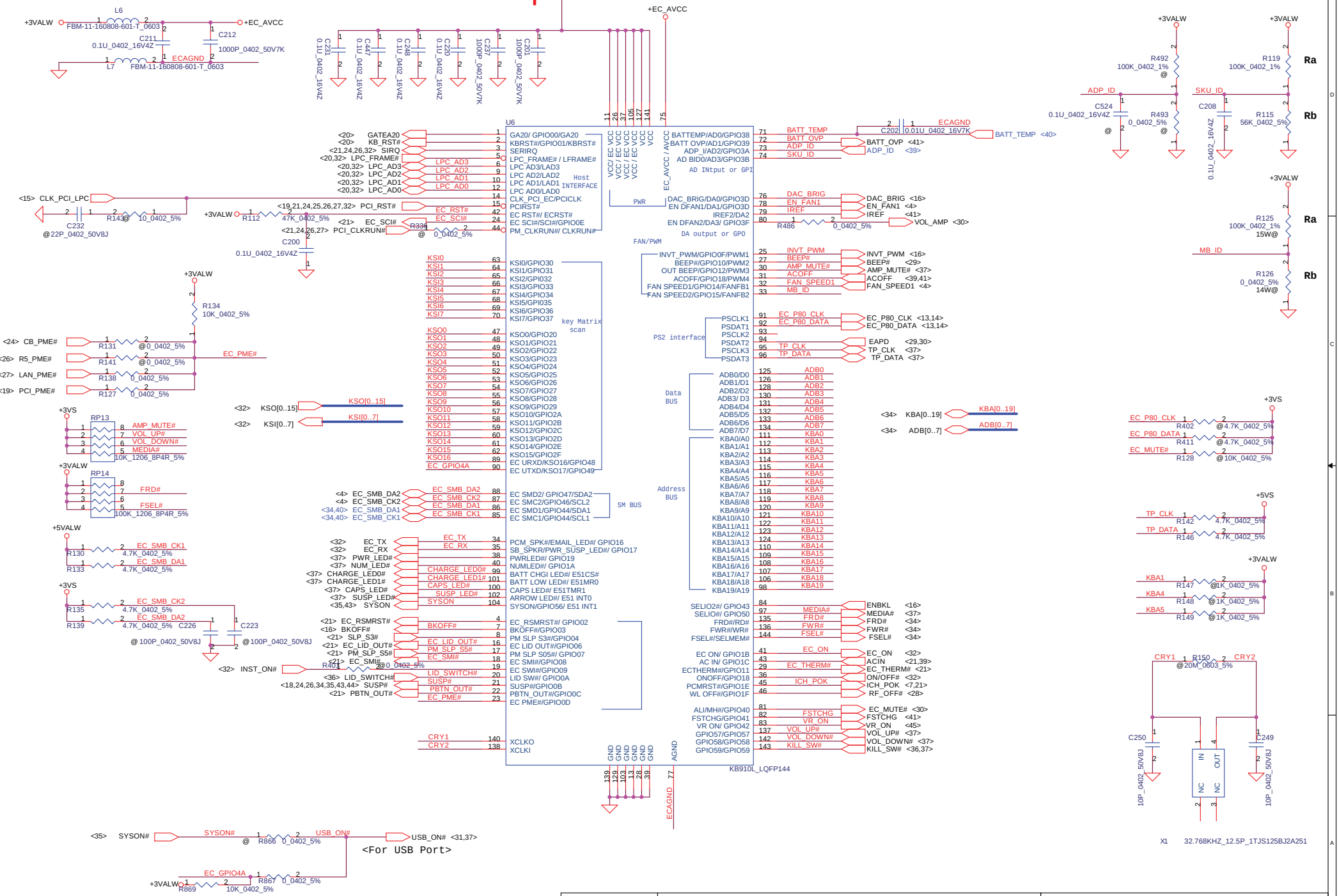
Analog Board ID definition,
Please see page 3.



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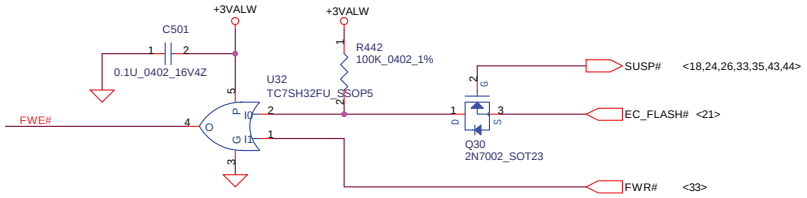

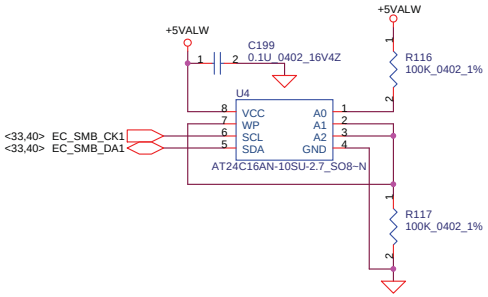

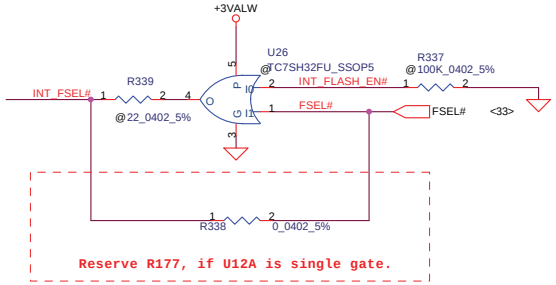

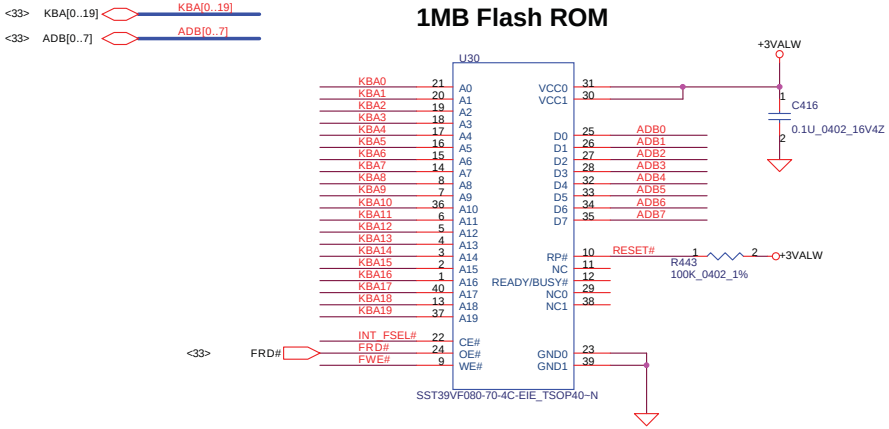

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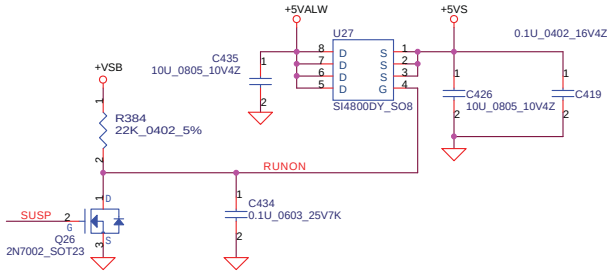
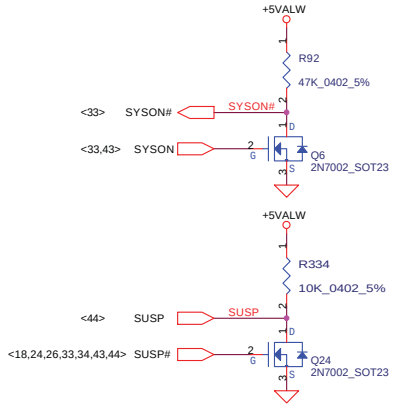
+5VALW to +5VS Transfer





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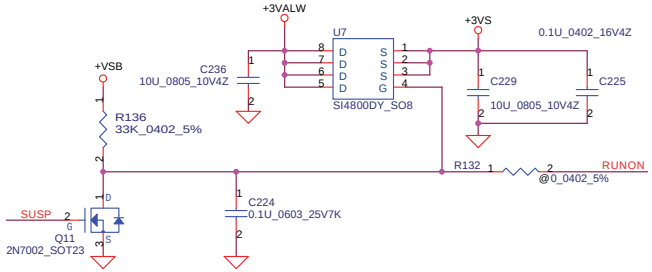

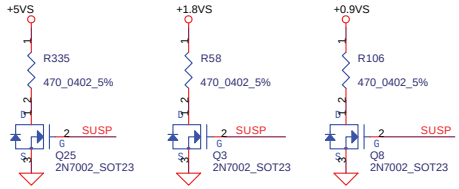

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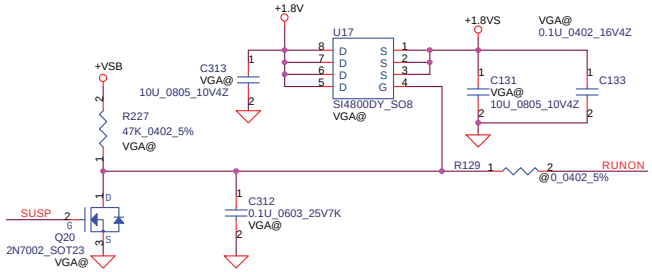

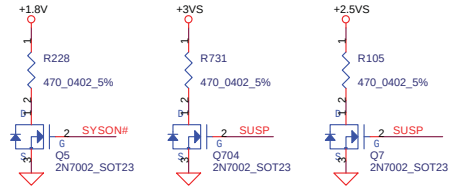

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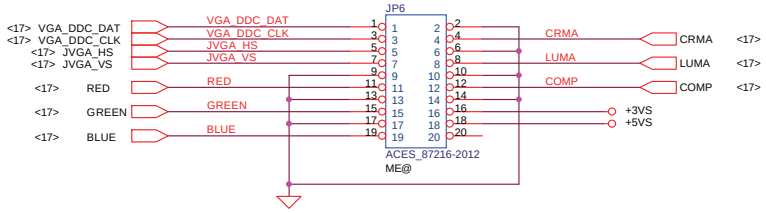
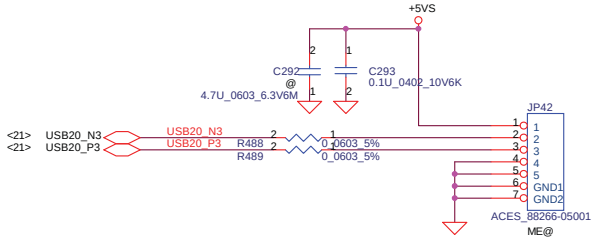
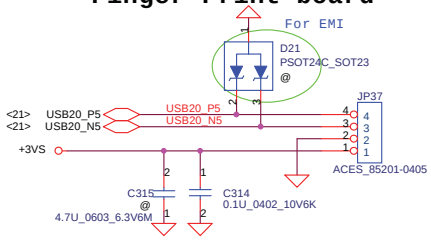
VGA I/O PORT Connector



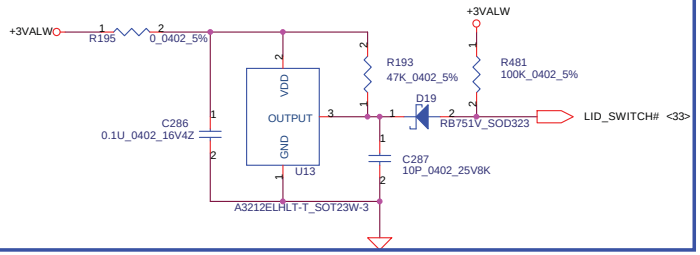
CMOS Camera Conn



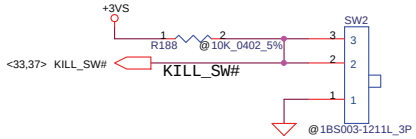
Finger Print board



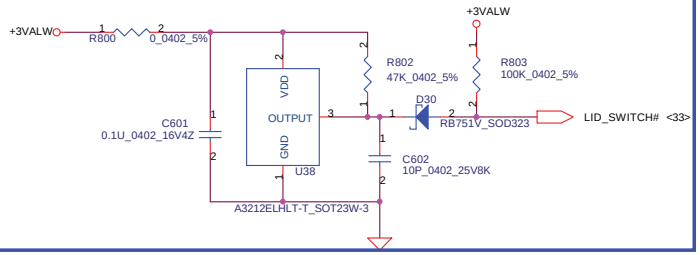
LID Switch (HDL00@)



Kill Switch



LID Switch 2 (HDL20@)



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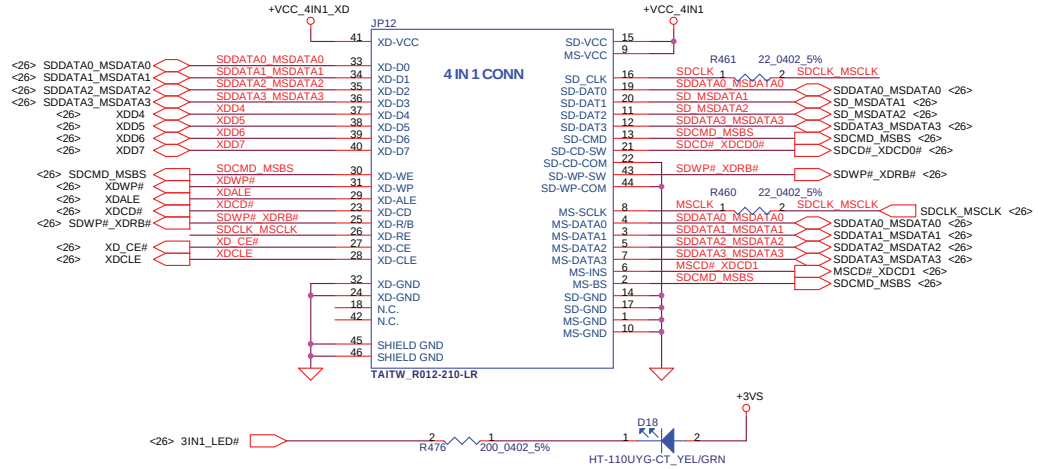
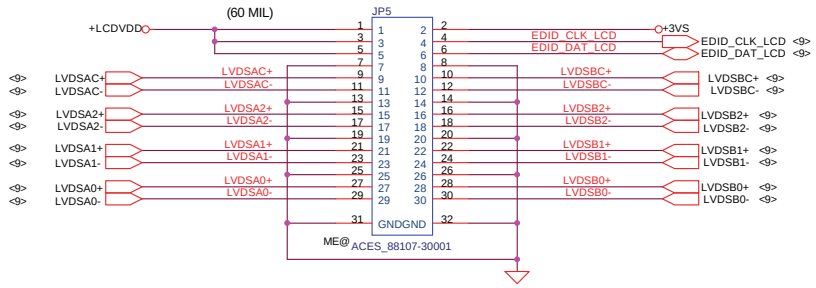
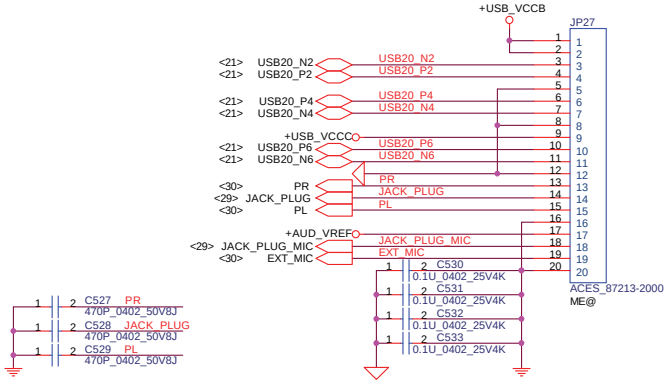
4 in 1 Card Reader

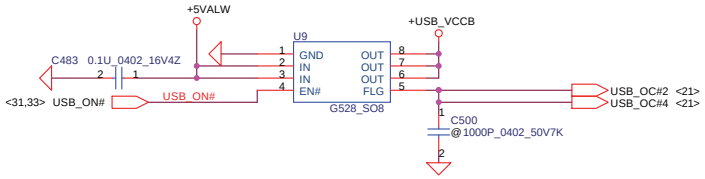


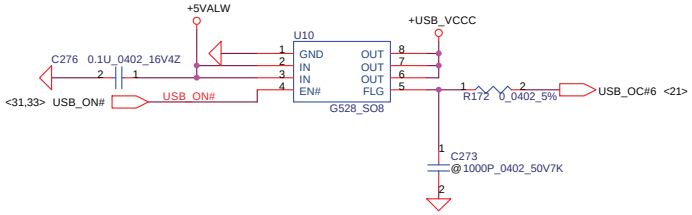
UMA LCD/PANEL Conn.



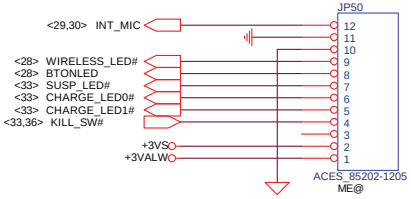
Audio Jack/USB Conn.



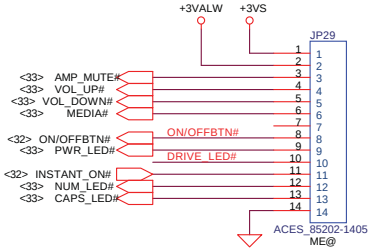


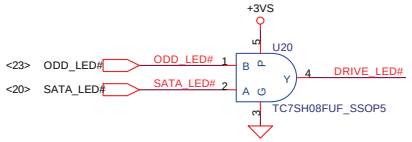


INST ON & LED

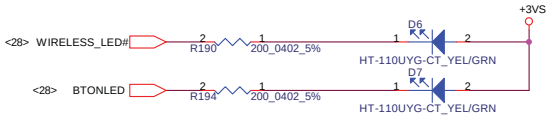


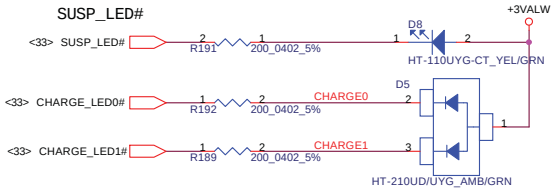
PWR ON/OFF SW & LED



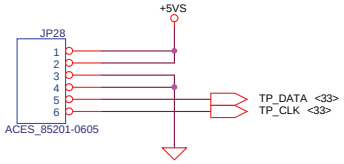


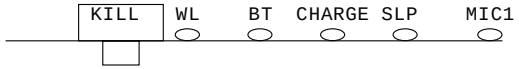
Front LEDs (HDL00@)





T/P Board





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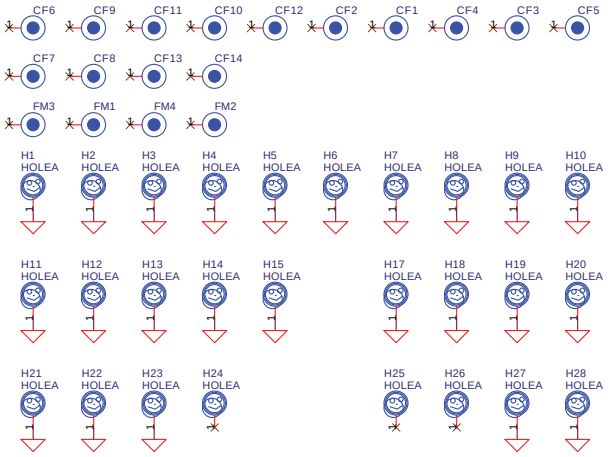

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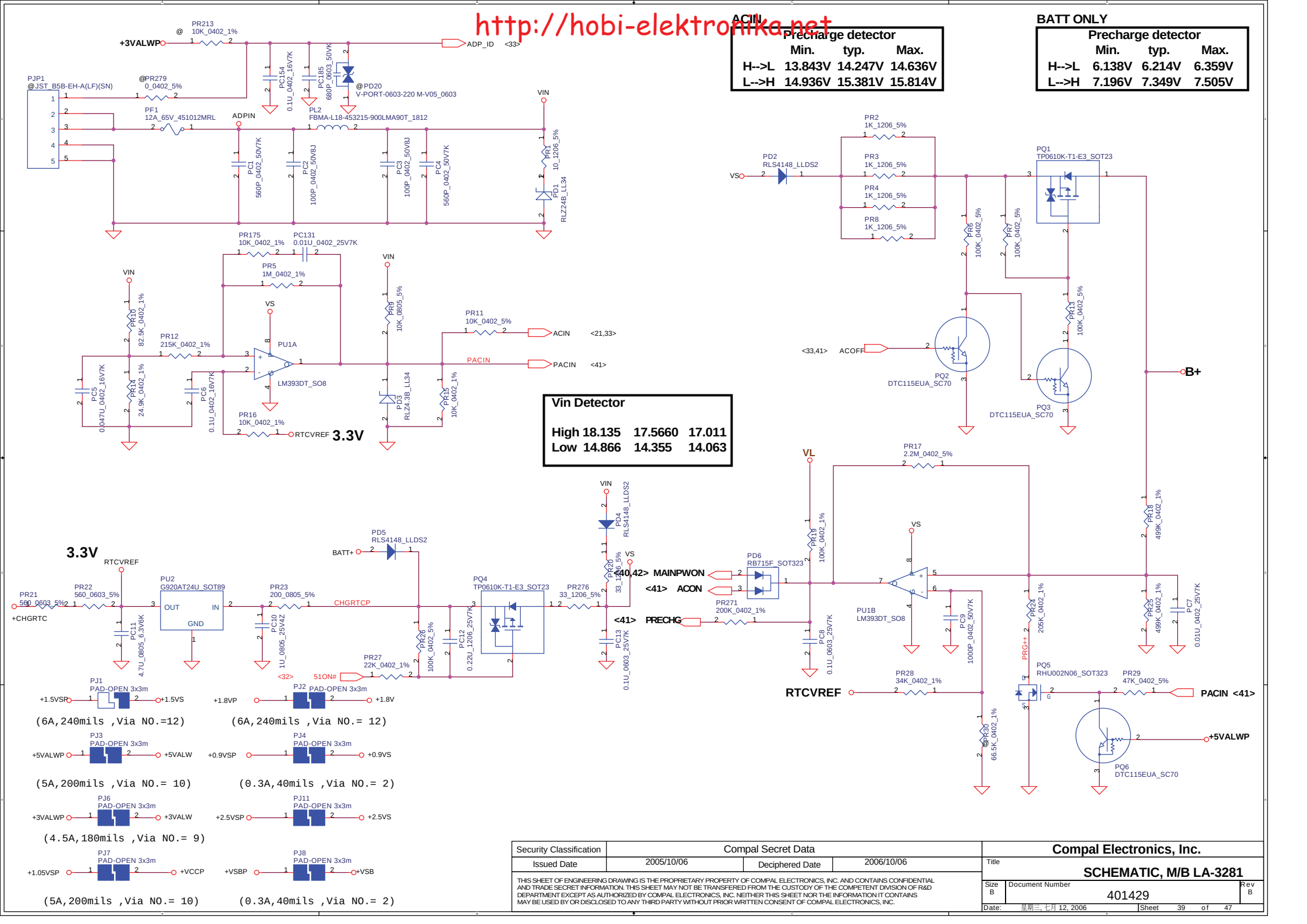

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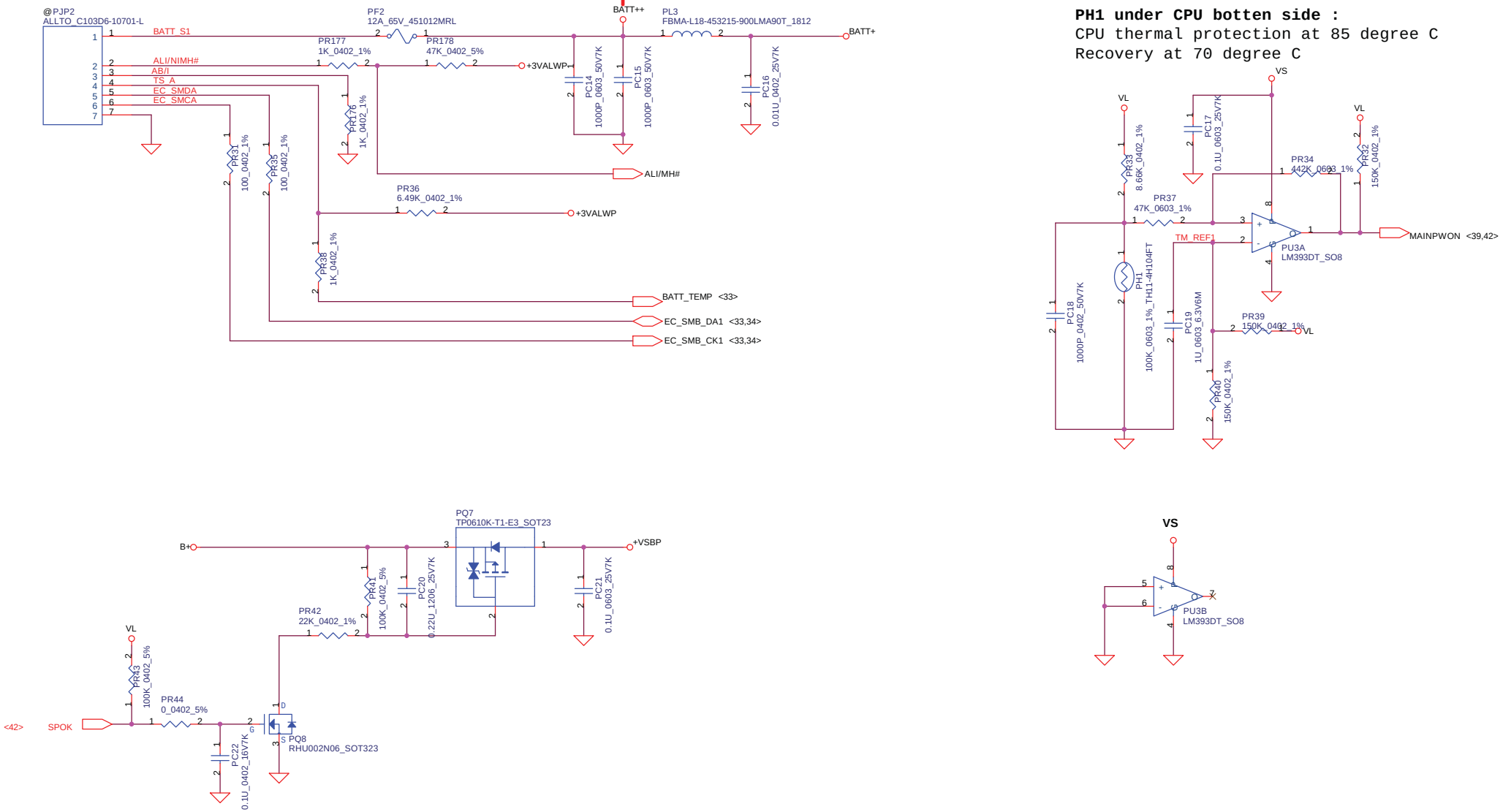
PH1 under CPU botten side :
CPU thermal protection at 85 degree C
Recovery at 70 degree C



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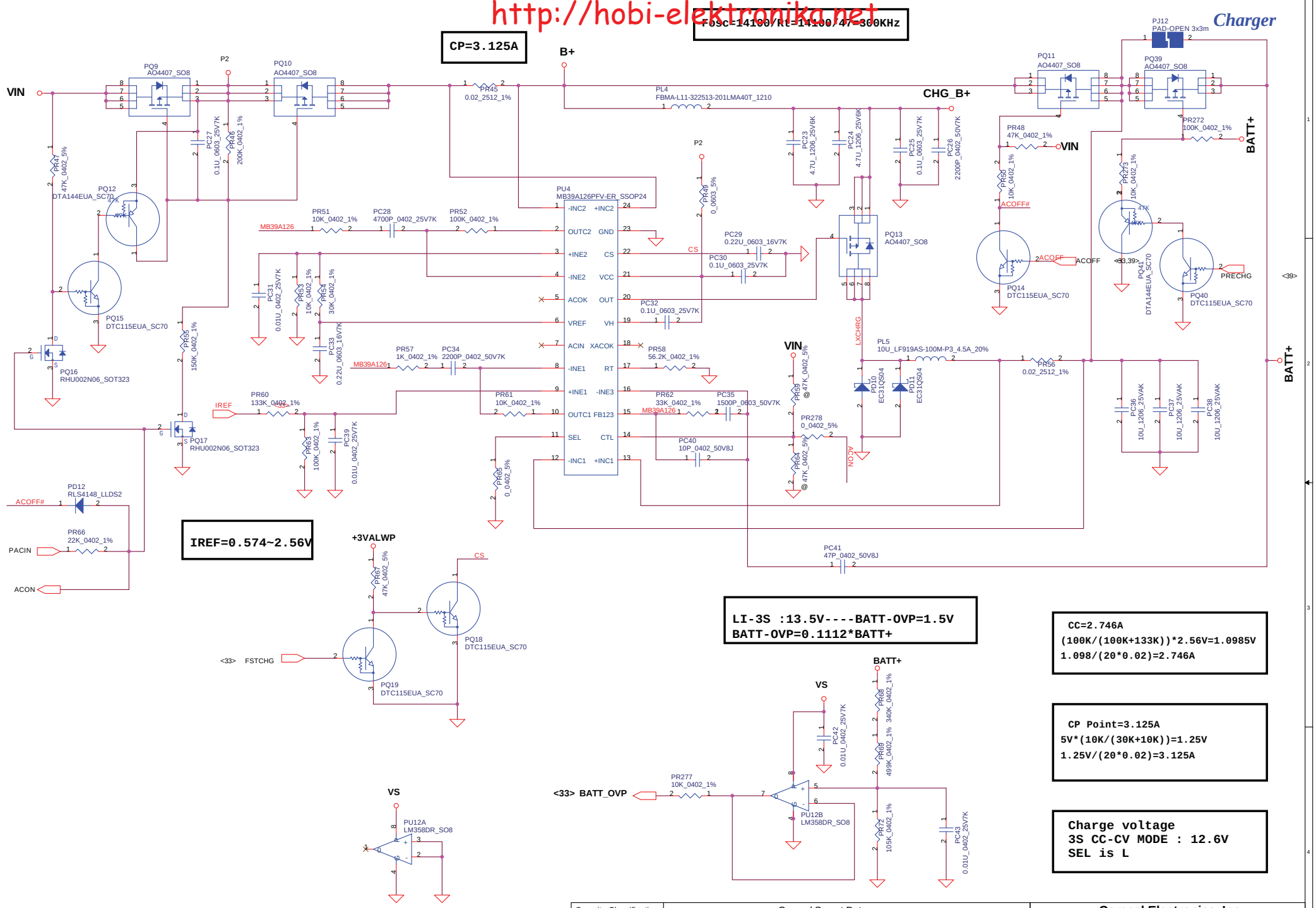
Charger



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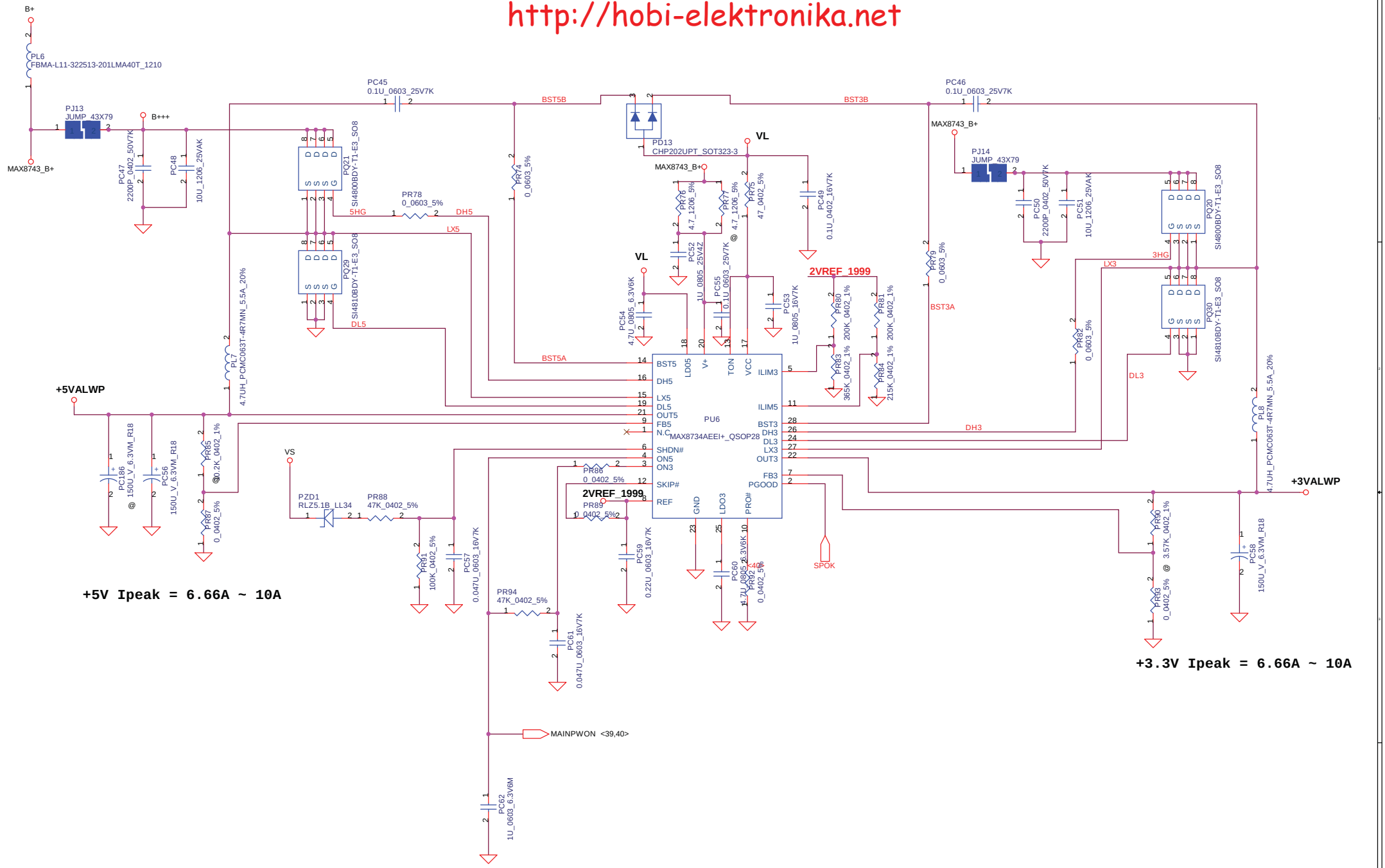

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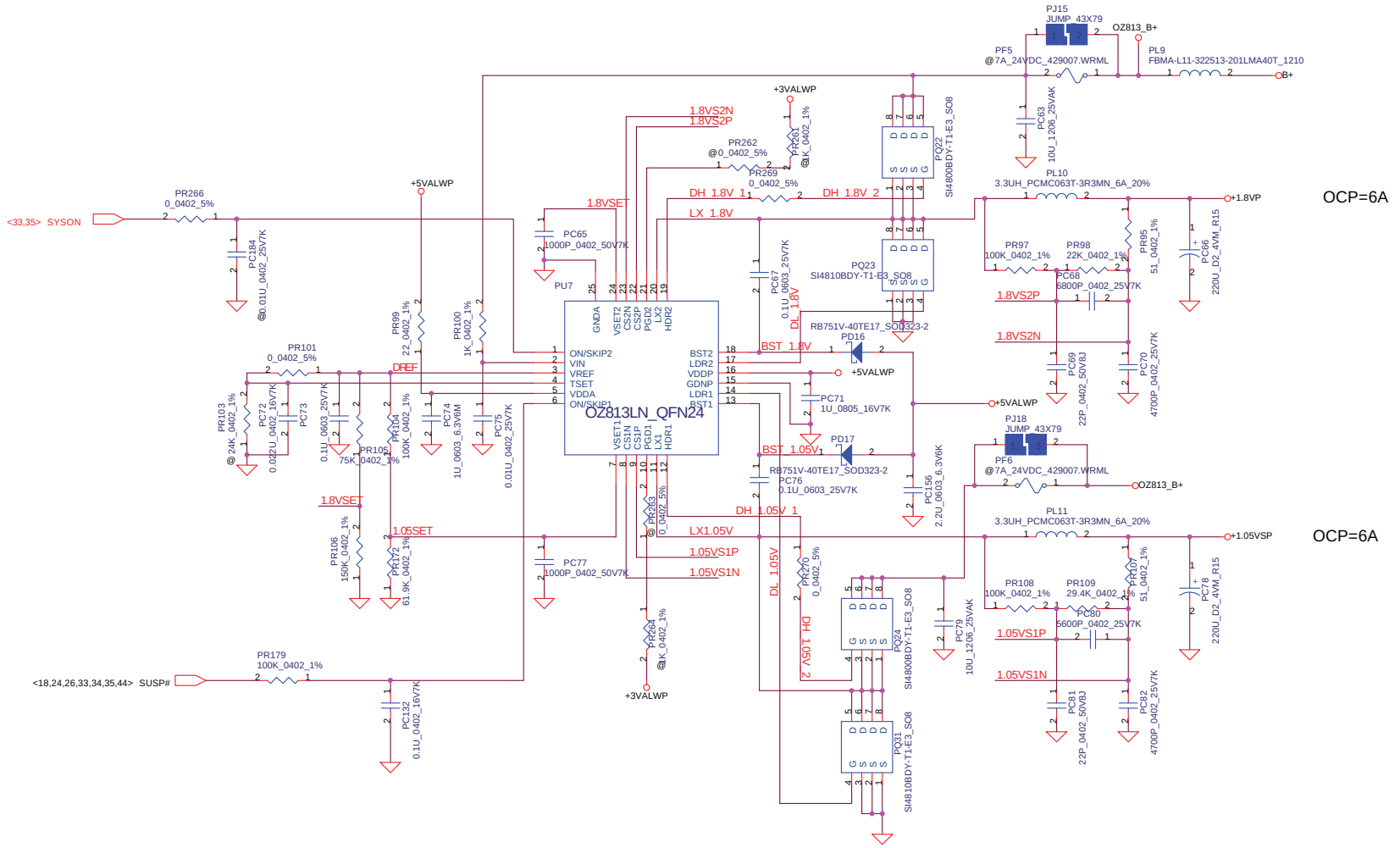

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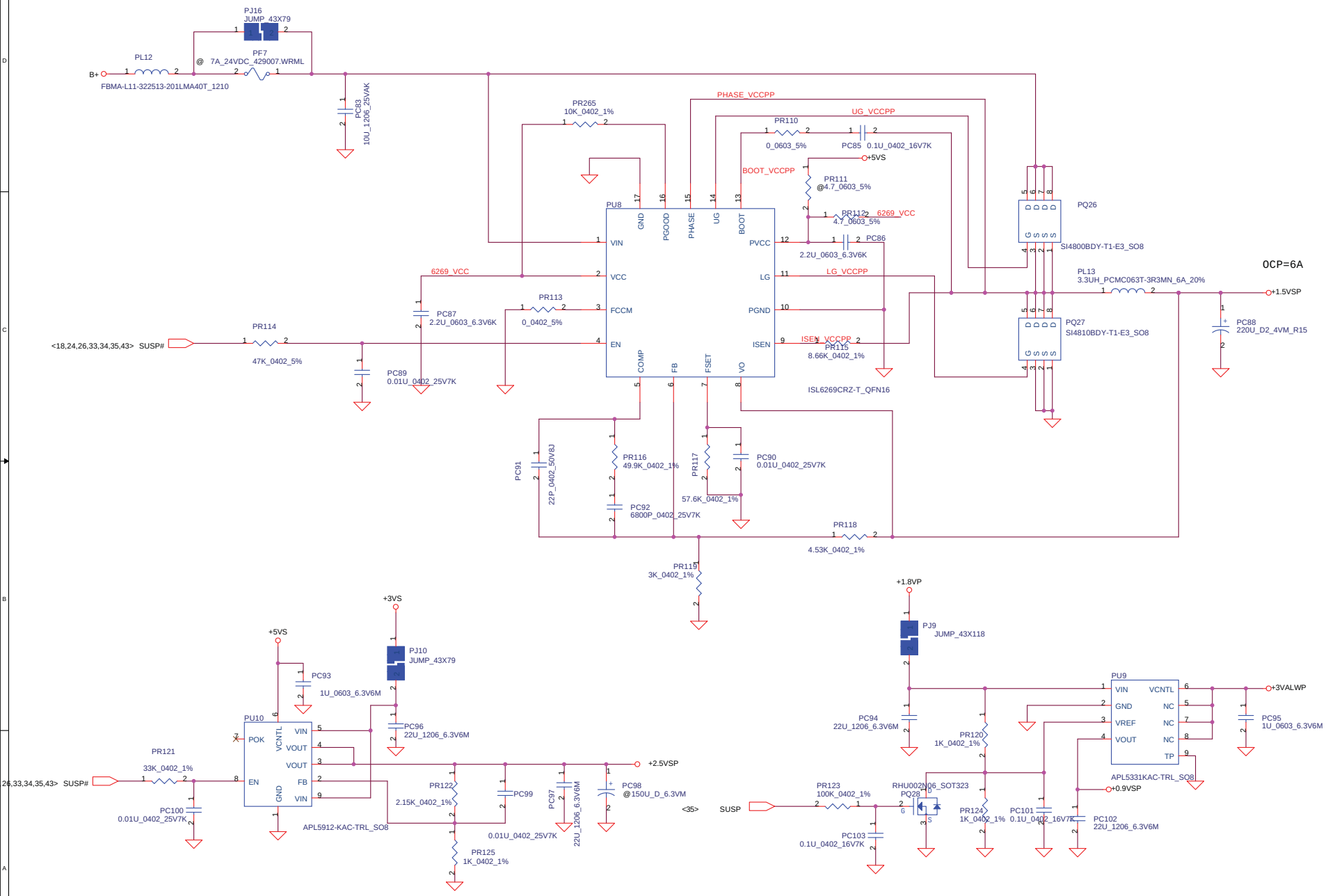

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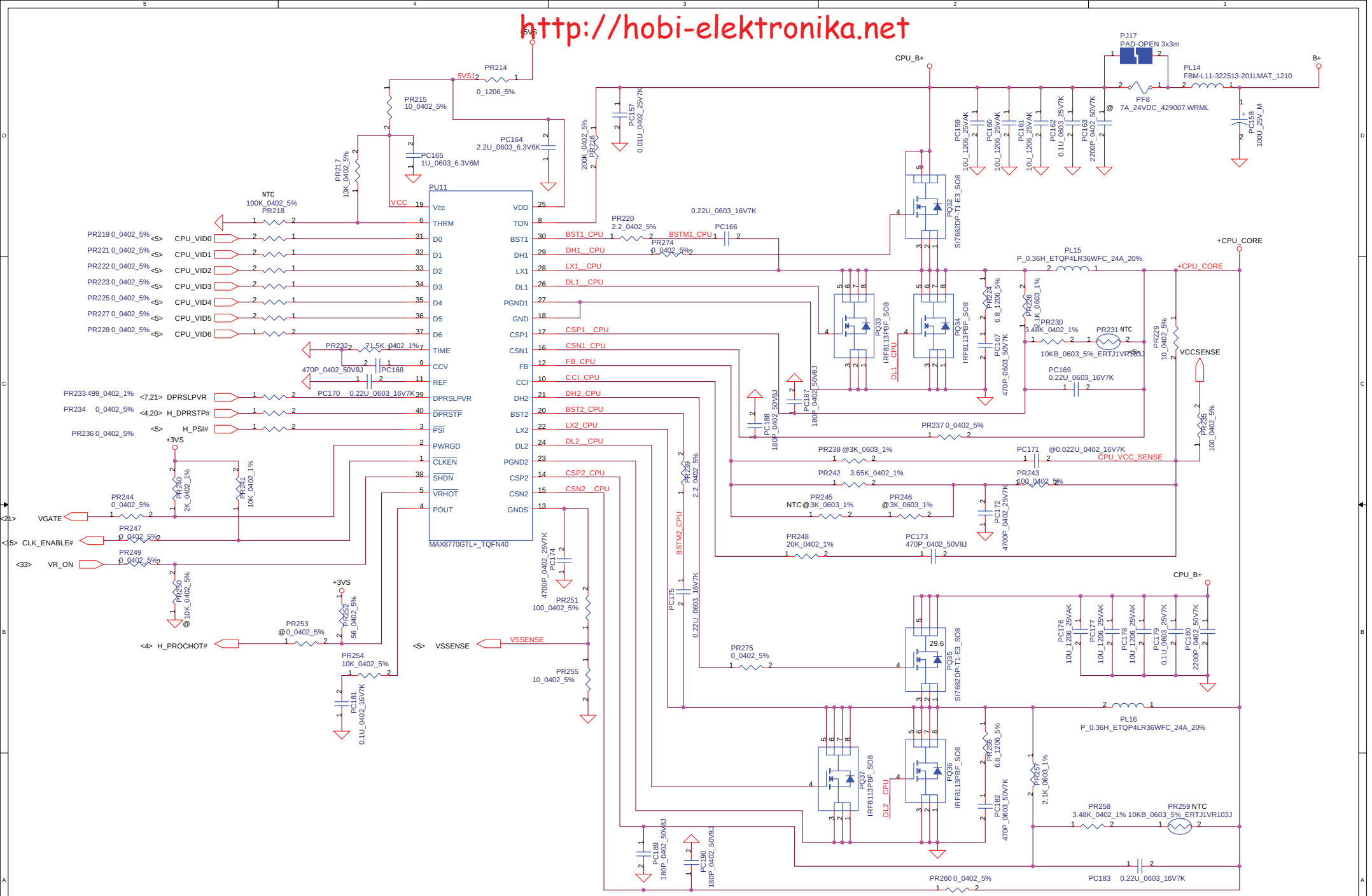

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Version change list (P.I.R. List)

Item	Fixed Issue	Rev.	PG#	Modify List	B.Ver#	Phase
1	Avoid leakage voltage and current to effect BATT_OVP signal	0.1	41	1.add PR277		
2	Add power consumption	0.1	41	1.Change external control signal to ACON 2.Add PR278		
3	For EMI request	0.1	39	1.add PR279		
4	Change recovery value is in order to adaptor voltage too low issue	0.1	39	1It .changed value of PR24 that 499k_0402 to 205k_0402		
5	It is order to reduce CPU core voltage inflence	0.2	45	Add pc187,pc188,pc189,pc190		

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Version change list (P.I.R. List)

Item	Fixed Issue/Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
A Test						
1	Copy schematic from HDL00					
2	Add 2nd BT connector	0.1	28	Add JP51,C60,Q706,Q705,Q708,R801,R810		
3	Add 2nd LID switch	0.1	36	Add U38,D30,R800,R802,R803,C601,C602		
4	Remove Front LEDs from MB	0.1	37	Del D6,D7,D8,D5,R190,R194,R191,R192,R189		
B Test						
5	Change audio solution from AD1986A to ALC861	0.2	29/30			
6	Add Front LEDs to MB(Reverse HDL00 Design)	0.2	37	Add D6,D7,D8,D5,R190,R194,R191,R192,R189		
C Test						
7	Sloving ICS pin 50, 51 no clock issue	0.3	15	Add R865 to U29.8 and grounded		
8	wake up on USB when AC-IN.	0.3	31, 33, 37	1. Add R866, R867 2. change EC pin 90 from KSO17 to EC_GPIO4A 3. connect R866, R867 pin2 together, and net name is USB_ON#. 4. change syson# to USB_ON#, and control U9, U10 and U25.		
9	EMI solution	0.3	16	1. change L14 from 0 ohm to bead 300 ohm 2. change C295 from 0.8pF to 470pF		
10						
11						
12						
13						
14						

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